Changjae Moon

Email: moonchangjae@postech.ac.kr | LinkedIn: linkedin.com/in/changjae-moon-259aa31b2 | Phone: +82-10-7353-9398

EDUCATION

Postdoctoral Researcher **Pohang University of Science and Technology (POSTECH)**, Korea *Mar. 2025−Present*

M.S.-Ph.D. Combined **Pohang University of Science and Technology (POSTECH)**, Korea *Mar. 2019−Feb. 2025*
Electrical Engineering, Advisor: Prof. Byungsub Kim, GPA: 3.95/4.3
Dissertation: "**Design of Compact and Energy-Efficient Inverter-based High-Speed Transmitter**"

B.S. **Pohang University of Science and Technology (POSTECH)**, Korea *Mar. 2014−Aug. 2018*
Electrical Engineering, GPA: 3.63/4.3

REASEARCH INTERESTS

High-speed electrical and optical wireline communication systems with focus on:

- Energy-efficient transceiver architectures for short-reach and chip-to-chip interconnects.
- Novel equalization techniques and signal processing for high-speed serial links.
- Optical modulator driver design.
- Compact single-ended transmitter/receiver design.
- PAM4 and high-order modulation schemes for bandwidth-efficient communication.

Proven track record with *ISSCC*, *ESSCIRC*, *JSSC*, *TCAS-I, TCAS-II, OJ-SSCS* publications and US patent.

PUBLICATIONS

Journal Papers (5 papers, 3 first-author)

[J1] **Changjae Moon**, Minsoo Choi, Myungguk Lee, and Byungsub Kim, "Review on Resistive Termination Techniques Driven by Wireline Channel Behaviors," ***IEEE Open Journal of the Solid-State Circuits Society (OJ-SSCS)***, vol. 4, pp. 305-317, Dec. 2024.

[J2] **Changjae Moon**, Iksu Jang, Sungmin Lim, Yaejoon Huh, and Byungsub Kim, "3 x 16 Gb/s Compact Single-ended PAM4 Transmitters with Inverter-based Crosstalk Compensation for Memory Interfaces," ***IEEE Transactions on Circuits and System II: Express Briefs (TCAS II)***, vol. 71, no. 12, pp. 4884-4888, Dec. 2024.

[J3] **Changjae Moon**, Jaeyoung Seo, Myungguk Lee, Iksu Jang, and Byungsub Kim, "A Single-Ended Inverter-based Addition-Only Feed-Forward Equalization Transmitter," ***IEEE Journal of Solid-State Circuit (JSSC)***, vol. 59, no. 11, pp. 3741-3751, Nov. 2024.

[J4] Myungguk Lee, Jaeik Cho, Junung Choi, Won Joon Choi, Jiyun Lee, Iksu Jang, **Changjae Moon**, Gain Kim, and Byungsub Kim, "Compact Single-ended Transceivers Demonstrating Flexible Generation of 1/N-rate Receiver Front-ends for Short-Reach Links," ***IEEE Transactions on Circuits and System I: Regular Papers (TCAS I)***, vol. 71, no. 1, pp. 373-382, Jan. 2024.

[J5] Jaeyoung Seo, Sooeun Lee, Myungguk Lee, **Changjae Moon**, and Byungsub Kim, "A 20-Gb/s/Pin Compact Single-Ended DCC-Less DECS Transceiver With CDR-Less RX Front-End for On-Chip Links," ***IEEE Journal of Solid-State Circuit (JSSC)***, vol. 58, no. 11, pp. 3253-3265, Nov. 2023.

Conference Papers (4 papers, 1 first-author at ISSCC)

[C1] **Changjae Moon**, Jaeyoung Seo, Myungguk Lee, Iksu Jang, and Byungsub Kim, "A 20 Gb/s/pin 1.18 pJ/b 1149um2 Single-Ended Inverter-based 4-tap Addition-Only Feed-Forward Equalization Transmitter with Improved Robustness to Coefficient Errors in 28nm CMOS," ***IEEE International Solid-State Circuits Conference (ISSCC) Dig. Tech. Papers***, pp. 450-451, Feb. 2022.

[C2] Jaeyoung Seo, Sooeun Lee, Myungguk Lee, **Changjae Moon**, and Byungsub Kim, "A 20-Gb/s/pin 0.0024-mm2 Single-Ended DECS TRX with CDR-less Self-Slicing/Auto-Deserialization to Improve Tolerance on Duty Cycle Error and Supply Noise for DCC/CDR-less Short-Reach Memory Interfaces," ***IEEE International Solid-State Circuits Conference (ISSCC) Dig. Tech. Papers***, pp. 456-457, Feb. 2022.

[C3] Jaehyun Ko, Iksu Jang, Chanho Kim, Jihoon Park, **Changjae Moon**, Sooeun Lee, and Byungsub Kim, "A 50 Mb/s Full HBC TRX with Adaptive DFE and Variable-Interval 3x Oversampling CDR in 28nm CMOS Technology for A 75 cm Body Channel Moving at 0.75 Cycle/sec", ***IEEE 48th European Solid-State Circuits Conference (ESSCIRC) Dig. Tech. Papers***, pp. 213-216, 2022.

[C4] Iksu Jang, Jaeyoung Seo, **Changjae Moon**, and Byungsub Kim, "A Cost-efficient FPGA-based Embedded System for Biosensor Platform", ***IEEE International SoC Design Conference (ISOCC)***, pp. 67-68, 2022.

RESEARCH EXPERIENCE

1. Next-Generation Optical Packaging Technology Development Project *July. 2025−Present*
Funded by the National Research Foundation of Korea

Project: Interposer Technology with Integrated Opto-Chiplets for CPO Based on 2.5D Optical Packaging
- Designing PAM4-100 Gbps single-channel MRR (micro-ring resonator) optical modulator driver.
- Developing enhanced modulation voltage swing of MRR optical modulator through differential AC coupling architecture and cascaded output driver topology.
- Implementing AC coupling structure with on-chip bias tee and enabling independent cathode/anode voltage control for MRR optical modulator.
- Applying Cherry-Hooper inverter-based amplifier architecture to achieve high-speed and high-linearity amplification in pre-driver stage.

2. Strategic Industry-Academia Collaboration Project *Sep. 2022−Sep. 2025*
Funded by Samsung Electronics Company Ltd.

Project: 16 Gbps Single-Ended Compact Transceiver
- Developed single-ended PAM4 transmitters with crosstalk compensation (XTC) for short-reach interfaces.
- Developed simple encoders and transition detectors to identify PAM4 data patterns causing crosstalk and activate inverter-based XTC taps.
- Minimized compensation error due to mismatch through gain and delay control of XTC.
- Published in *IEEE Transactions on Circuits and System II: Express Briefs (TCAS-II)* 2024 [J2].

3. Design and Application of Next-Generation Non-Volatile Memory Hierarchy Cluster Academia Collaboration Program Funded by Samsung Electronics Company Ltd. *July. 2021−June. 2024*

Project: Inverter-Based Compact 4-Tap FFE Transmitter Development for Next-Generation Non-Volatile Memory
- Developed novel addition-only FFE (A-FFE) architecture that produces equivalent output to conventional FFE.
- Developed A-FFE to completely eliminate subtractions between FFE taps, enabling the use of inverter drivers as FFE taps.
- Reduced unnecessary power consumption from tap subtractions and achieved robustness to quantization errors of tap coefficients through channel loss suppression of error signals.
- Presented in *IEEE International Solid-State Circuits Conference* (*ISSCC*) 2022 [C1] and published in *IEEE Journal of Solid-State Circuits* (*JSSC*) 2024 [J3].
- Registered with a U.S. patent [P1] and awarded in Korea Semiconductor Design Contest (Corporate Special Awards) [A2].

PATENT

[P1] FEED FORWARD EQUALIZER AND SYSTEM INCLUDING THE SAME (No. US12119963B2) *Oct. 2024*

HONORS AND AWARDS

[A1] Corporate Special Awards at the Korea Semiconductor Design Contest *2023*

[A2] Corporate Special Awards at the Korea Semiconductor Design Contest *2022*

EXPERIENCES

Military Service **Alternative Military Service as Technical Research Personnel** *Mar. 2023−Feb. 2026 (expected)*

Teaching Assistant **Pohang University of Science and Technology (POSTECH)**, Korea *Mar. 2019−July. 2019*
Basic Circuit Experiments (EECE 281)

TECHNICAL SPECIALTIES

Interconnect Modeling and Characterization
- The electrical and optical modeling and characterization of various high-speed interconnects.

High-Speed I/O Circuit Design
- Low-power, high-speed transmitters, receivers, FFE, DFE, CTLE, PLL, CDR, and clock distribution circuits.

On-Chip Measurement and Testing Methodology
- Design of on-chip measurement and testing circuit such as on-chip bit-error-rate-testers (BERTs), PRBS generators, and eye monitoring circuits.
- Implementation of on-board testing systems based on FPGA and PC.

SKILLS

Technical Skill Programming Languages: C/C++ language and Python
Circuit Simulation Tools: HFSS, EMX, Cadence, Verilog, SPICE and MATLAB & Simulink
Synthesis tool: Design compiler and IC compiler
PCB tool: PADS

Languages Korean, English

REFERENCES

Prof. Byungsub Kim Professor in Department of Electrical Engineering
Pohang University of Science and Technology (POSTECH), Pohang, South Korea
Email: byungsub@postech.ac.kr, Phone: +82-54-279-2382

Prof. Jae-Yoon Sim Professor in Department of Electrical Engineering
Pohang University of Science and Technology (POSTECH), Pohang, South Korea
Email: jysim@postech.ac.kr, Phone: +82-54-279-2378

Prof. Ho-Jin Song Professor in Department of Electrical Engineering
Pohang University of Science and Technology (POSTECH), Pohang, South Korea
Email: hojin.song@postech.ac.kr, Phone: +82-54-279-2378