A 50 Mb/s Full HBC TRX with Adaptive DFE and Variable-Interval 3x Oversampling CDR in 28nm CMOS Technology for A 75 cm Body Channel Moving at 0.75 Cycle/sec

Jaehyun Ko[1], Iksu Jang[1], Chanho Kim[1], Jihoon Park[1], Changjae Moon[1], Sooeun Lee[2] and Byungsub Kim[1]

[1]Department of Eletrical Engineering, Pohang University of Science and Technology (POSTECH), Pohang, Korea,
[2]Samsung Electronics, Hwaseong, Korea,
E-mail: byungsub@postech.ac.kr

Abstract—This paper reports a 50 Mb/s full human body communication (HBC) transceiver (TRX) that communicates through a 75 cm body channel moving at speed of 0.75 cycle/sec. For the first time, adaptive decision feedback equalization (DFE) and a clock and data recovery (CDR) were integrated in a HBC TRX to adapt to a moving body channel in real time. In the proposed design, the transmitter (TX) consists of inverter-based driver that transmits non-return-to-zero (NRZ) signal to human body. The receiver (RX) utilized a 10-tap adaptive DFE to compensate for time-varying inter symbol interferences (ISIs) of moving body channel. Also, for clock synchronization, variable-interval 3x oversampling CDR (VI-3x-CDR) was adopted to overcome wide and asymmetric data-dependent jitter (DDJ). A test chip was fabricated in 28 nm CMOS technology. Compared with the prior arts that were measured with moving body channel, the data rate and the area were improved by 10x and 3x, respectively.

I. INTRODUCTION

As the number of connectivity around human body is enormously increasing for medical and entertainment purposes, energy efficient (long battery time) and high-speed (high quality of data) wearable and implantable devices are increasingly demanded. For those devices, early developed IEEE standards (802.15 task group) were established for the general connection of personal device at short distance: ZigBee (802.15.4), Bluetooth (802.15.1) and Ultra-wide band (UWB, 802.15.3). However, the power efficiency and data rate of these schemes were limited because the RF signal that broadcasts to air around the body suffers huge channel loss. To overcome such fundamental limitations, human body communication (HBC) which utilizes human body as communication medium is getting increasing attention because of the low channel loss of a human body channel [1], [4]-[7] as a promising solution for energy-efficient and high-speed wearable and implantable
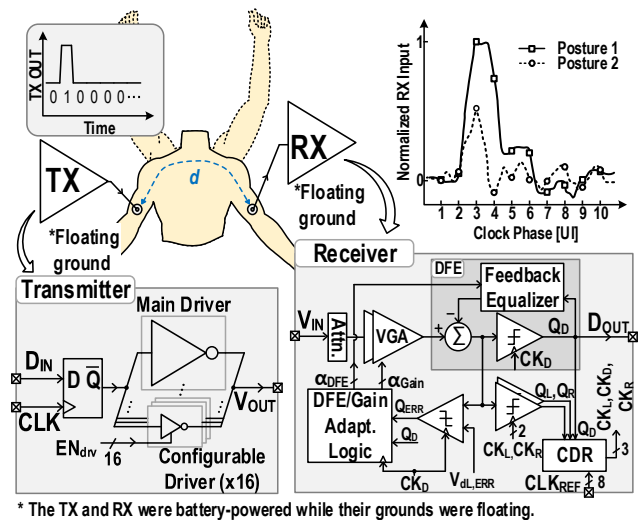

Fig. 1. An overall block diagram of the proposed HBC transceiver and SBRs measured with two different postures.

devices. In the past years, many researcher have focus on increasing the maximum speed of HBC TRX. The data rate of state-of-the-art HBC TRXs have reached over tens of Mb/s [1],[7]. However the achievable speed of HBC drastically drops with human motion because the electrical response of the body channel varies a lot with posture change. There have been some prior works that attempted to address this problem [4]-[6]. Reference [4] presented the first magnetic field HBC (mHBC) that achieved maximum data rate of 5 Mb/s while walking. As the inductances of coils at TX and RX vary with posture change, a frequencylocked-loop was adopted to maintain LC resonance frequency by tuning capacitance. However, channel variation by inductor mis-alignment by posture change and large coil area are still in issue. In electric field HBC (eHBC), prior works [5]-[6] tried to mitigate channel variation due to variable ground effect in which the capacitively-coupled return path varies.

The eHBC channel gain is determined by both the body path and the return path. P-OFDM HBC TRX [5] compensated for the channel variation with reconfigurable gain LNA by
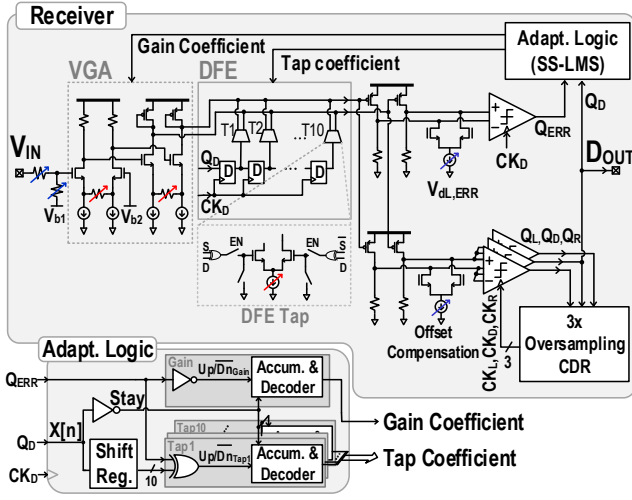
Fig. 2. A schematic diagram of the RX DFE datapath.

Fig. 3. A block diagram of the CDR and relevant simulations (an eye diagram and a jitter histogram).

continuously monitoring RC time constant of channel, which is associated with the channel status. However it only achieved the maximum data rate of 2 Mb/s while shaking head. It also occupied large area because of a huge OFDM modulation blocks. The work reported in [6] adopted resonance-matching technique in which the channel gain is automatically adjusted by changing inductance. It achieved the maximum data rate of 4 Mb/s, and showed that the channel gain was maintained for various distances between TX and RX. However, a large inductance is a big problem in implementation. Therefore, so far, no HBC TRX faster than 5 Mb/s has been demonstrated with a moving human body.

In this paper, we report a 50 Mb/s full human body communication (HBC) transceiver (TRX) that communicates through a 75 cm body channel moving at speed of 0.75 cycle/sec. To maintain high data rate with a quickly moving body channel, adaptive decision feedback equalization (DFE) and a clock and data recovery (CDR) were integrated in a HBC TRX for the first time. In experiment, the proposed TRX achieved 50 Mb/s with a body channel moving at the speed of 0.75 cycle/sec. This paper organized as follow. In section II, the proposed circuit design is explained. In section III, the measurement setup and the results are presented, and section IV discusses the results.

II. THE PROPOSED DESIGN

A. Overall architecture

The proposed HBC TRX consists of an inverter based TX and an adaptive DFE RX with a variable gain amplifier (VGA) and a variable-interval 3x oversampling CDR (VI-3x-CDR) (Fig. 1). The TX driver consists of a main driver (a large inverter) and 16 configurable driver (small inverters) that can be digitally controlled to adjust driving strength. By using this driver, baseband NRZ signal is transmitted through a body. In the RX, DFE cancels intersymbol interference (ISI) (Fig. 1) caused by the channel distortion which is the main obstacle in tens-of-Mb/s HBC [1]. Because two single-bit responses (SBRs) measured with two different postures greatly differ
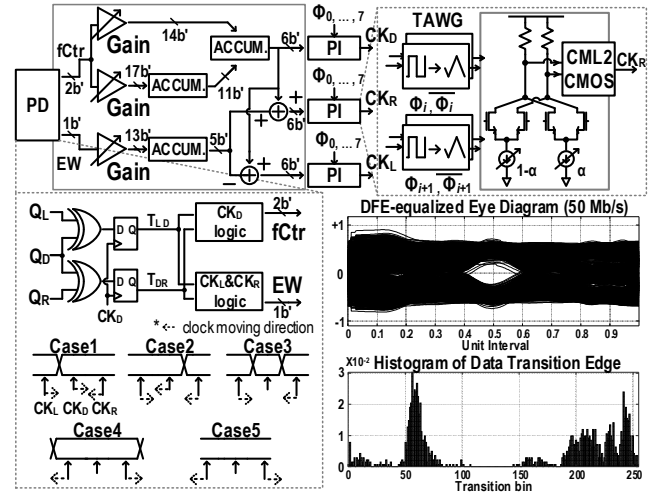
from each other (Fig. 1), DFE/CDR adaptation is necessary to body movement. For VGA/DFE adaptation, the sign-sign least mean square (SS-LMS) algorithm [3], which is widely used in high-speed wireline, was adopted for its good performance and efficiency. For CDR adaptation, VI-3x-CDR [2] was adopted for reliable operation. The finite-state machines (FSMs) for DFE/CDR adaptation were synthesized for the full-rate clock frequencies up to 50 MHz. Because human motion is much slower, the FSMs can continuously track time-varying characteristics of a moving body channel.

B. Receiver DFE datapath circuit

The RX employs a full-rate 10-tap current-summing DFE adopted from [1] (Fig. 2). In HBC, the channel gain varies a lot depending on the channel distance and the data rate. Also, the input common-mode voltage may fluctuate. Under such circumstances, keeping the linearity of the analog circuits is challenging. The input gain is controlled by a two-stage VGA and a programmable voltage-dividing termination to keep the linearity of the circuits. Also, a multi-stage topology using current mirrors provides a wide linear operation range. The 10 DFE taps cancel 10 post-cursor ISIs. The two output amplifiers of the DFE summer have threshold control knobs. One cancels the datapath offset for data sampling (DFE output: $Q_D = D_{OUT}$) and edge sampling (left: Q_L, right: Q_R). The other one subtracts the desired signal level ($V_{dL,ERR}$) for error sampling (Q_{ERR}). Q_D, Q_L, and Q_R are used in CDR adaptation [2]. DFE adaptation uses Q_D and Q_{ERR}. In the adaptation logic, update steps and cycles can be reconfigured to adjust adaptation bandwidth depending on channel circumstances.

C. Variable-interval 3x oversampling CDR

VI-3x-CDR [2] was adopted and modified for the proposed CDR based on phase interpolators (PIs). Because the SBR's ISI tail is large and longer than the DFE tap count (Fig. 1), the ISIs left after the DFE subtraction are not negligible, causing large and complex data-dependent jitter. Fig. 3 shows simulation results after the DFE compensation. The eye width is only 0.2 UI. The jitter histogram is widely dispersed in an
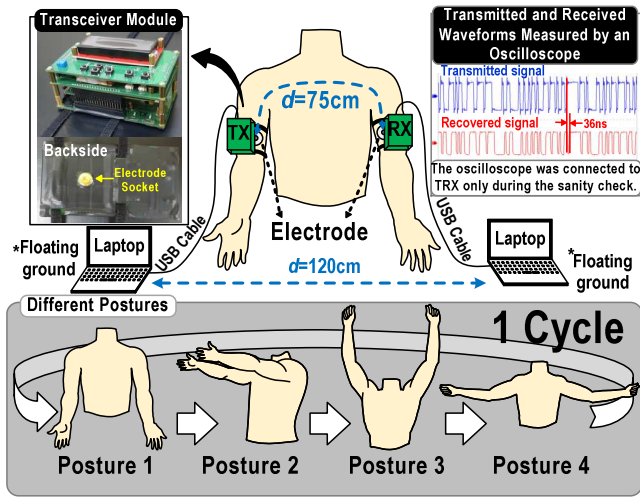
Fig. 4. Measurement setup and postures.

BER Measurement without Motion at 50 Mb/s

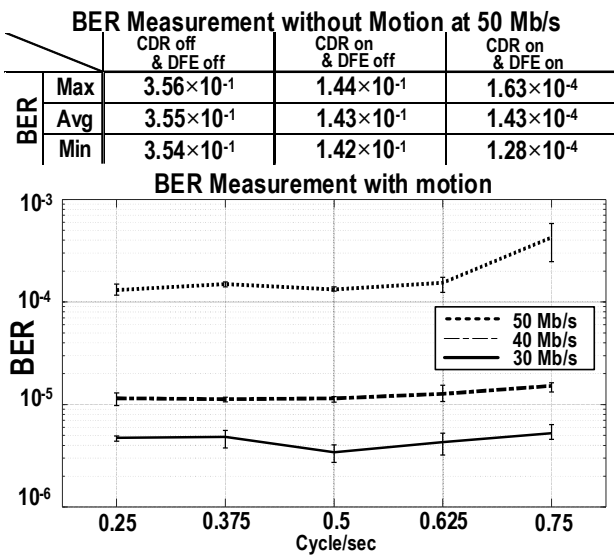|		CDR off & DFE off	CDR on & DFE off	CDR on & DFE on
BER	Max	3.56×10^{-1}	1.44×10^{-1}	1.63×10^{-4}
	Avg	3.55×10^{-1}	1.43×10^{-1}	1.43×10^{-4}
	Min	3.54×10^{-1}	1.42×10^{-1}	1.28×10^{-4}

Fig. 5. BER measurements with a 75-cm body channel.

asymmetric irregular shape that has many peaks, and is also severely skewed from the typical edge locations (0.5 UI apart from the center of the eye diagram). Therefore, a typical CDR cannot work with this body channel because it usually locates the data clock (CK_D) 0.5 UI apart from the average phase of the jitter distribution. On the other hand, the VI-3x-CDR adjusts the edge clocks (CK_L and CL_R) to track the edges of the data eye rather than tracking the jitter density while placing the data clock (CK_D) in the middle of the two edge clocks [2]. Therefore, the VI-3x-CDR samples the center of the eye irrespective of the magnitude and shape of the jitter [2]. Fig. 3 conceptually describes the proposed CDR behavior. If only one transition occurs (Case 1: $Q_L \neq Q_D = Q_R$, or Case 2: $Q_L = Q_D \neq Q_R$), the CDR tries to increase (Case 1) or to decrease (Case 2) the CK_D phase while trying to reduce the phase difference between CK_L and CK_R. If two transitions occur (Case 3: $Q_L \neq Q_D \neq Q_R$), the CDR tries to reduce the phase difference between CK_L and CK_R without changing CK_D. If no transition
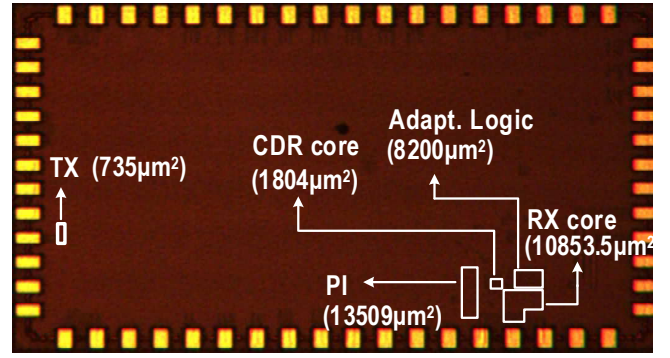

Fig. 6. A Microphotograph of the chip.

is detected five times consecutively (Case 4 and Case 5: $Q_L = Q_D = Q_R$), the CDR tries to increase the phase difference between CK_L and CK_R without changing CK_D. For this adaptation, phase detectors (PDs) generate two control signals: 1) fCtr to control CK_D phase and 2) EW to control the phase difference between CK_L and CK_R. fCtr and EW are fed to digital filters to produce the phase codes, from which three PIs generate CK_D, CK_L, and CK_R using 8-phase clocks ($\Phi_0 \ldots \Phi_7$) to sample Q_D, Q_L, and Q_R, respectively. The PI adopted typical current mode topology with resistive load, and tri-angular wave generators (TAWG) which consists of digitally configurable current-starving inverters and a MOS capacitor bank were placed before the interpolation to keep phase linearity at wide range of clock speed. Except PIs and samplers, the CDR was fully synthesized.

III. EXPERIMENT RESULTS

A. Measurement setup

The TRX was fabricated with an on-chip bit error rate tester (BERT) circuit in 28 nm CMOS (Fig. 6). Two test modules of the TX and the RX were configured and separately powered by two different battery-powered laptops with floating grounds to avoid ground coupling through the power/USB cables (Fig. 4). An electrode on the backside of a module directly contacts the body without a lead wire (Fig. 4). The test modules were tied to upper arms with straps for stable contact during the test. The TX and the RX communicated through a 75 cm body channel. The waveforms of the transmitted and received bit patterns were measured with an oscilloscope for a sanity check before the quantitative bit error rate (BER) measurement. The measured bit patterns were identical (Fig. 4). The oscilloscope was used only during the sanity check, and then disconnected from the TRX during the BER measurement to avoid ground coupling via power cables.

B. Experiment results

BER was measured multiple times by the on-chip BERT with and without body channel movement in various conditions. The BER measurements at 50 Mb/s with a motionless 75-cm body channel are reported in Fig. 5. When either DFE or CDR was disabled, the BER remained higher than 10^{-1}. When both DFE and CDR were enabled, the BER dropped to 1.43×10^{-4}, verifying that DFE and CDR play critical

215

TABLE I
PERFORMANCE SUMMARY AND A COMPARISION TABLE

		This work	ISSCC'19 [4]	JSSC'17 [5]	ASSCC'19 [6]	VLSI'17 [1]	VLSI'19 [7]
Process		28 nm	65 nm	65 nm	180 nm	65 nm	180 nm
Supply voltage		TX: 1.2 V, RX: 1 V	0.6 V	1.1 V	0.8 V	N/A	1 V
HBC Technique		Capacitive	mHBC	Capacitive	Capacitive	Capacitive	Galvanic
Communication Scheme		NRZ	OOK	8 P-OFDM BPSK	OOK	NRZ	Bipolar RZ
Data Rate		30 - 50 Mb/s	5 Mb/s	200 Kb/s -2 Mb/s	4 Mb/s	150 Mb/s	100 Mb/s
BER		$< 10^{-3}$	No BER measurement with moving body channel	$< 10^{-7}$	$< 10^{-5}$	$< 10^{-6}$	$< 10^{-9}$
Channel Distance		75 cm	100 cm	10 cm	150 cm	20 cm	A few cm
Human Motion While Testing		0.75 cycle/sec of pre-defined motion	While walking	While shaking head	Changing ground path distance from 2 cm to 20 cm	No motion	No motion
Adaptation		Yes	Yes	Yes	Yes	No	No
Area [mm^2]		0.036	0.12	0.542	2.8	0.00558	N/A
Energy Efficiency [pJ/bit]	TX	33.72	7.15	435	30	3.3	4.75
	RX	68.84	4.7	550	41	13.3	26.8
	Total	102.56	11.85	985	71	16.6	31.55

roles in overcoming the channel distortion and in timing recovery, respectively. The BER measurements with a 75-cm moving channel in various conditions are plotted in the min-max chart (Fig. 5). For precise measurement, the human subject repeated the cycle of four postures in Fig. 4 while the movement speed was adjusted to the beat of a metronome. At the fastest motion speed of 0.75 cycle/sec, the worst BERs were measured 6.36×10^{-6}, 1.63×10^{-5}, and 5.84×10^{-4} at the data rates of 30, 40, and 50 Mb/s, respectively (Fig. 5). In all test conditions (data rate: 30-50 Mb/s, motion speed: 0.25-0.75 cycle/sec), the measured BER remained smaller than 10^{-3}, verifying that DFE and CDR successfully adapted to the channel.

IV. DISCUSSION

The proposed HBC TRX achieved the maximum data rate of 50 Mb/s through a 75 cm body channel moving at speed of 0.75 cycle/sec for the first time while consuming 5.1 mW (102.5 pJ/b) and occupying only 0.036mm^2. Compared with the prior state-of-the-arts that were measured with moving body channels [4]-[6], the proposed TRX improved the maximum data rate by 10x at costs of 3x smaller area and reasonable energy consumption. Comparing the results at similar BERs reported in [5] and [6], our TRX achieved much faster data rates of 30 Mb/s and 40 Mb/s at costs of slightly higher BERs of 6.36×10^{-6} and 1.63×10^{-5}, respectively. The prior works that were not measured with moving body channels achieved much faster speeds of 100 Mb/s [7] and 150 Mb/s [1]. However, comparing our work with them is not fair because the achievable maximum data rate greatly decreases with a human motion. It is also noticeable that the proposed TRX has an advantage in area efficiency with technology scaling because it has a large portion of digital circuits and does not require bulky analog elements like inductors or analog filters.

REFERENCES

[1] J.-H. Lee, K. Kim, M. Choi, J.-Y. Sim, H.-J. Park, and B. Kim, "A 16.6-pJ/b 150-mb/s body channel communication transceiver with decision feedback equalization improving> 200% area efficiency," in 2017 Symposium on VLSI Circuits. IEEE, 2017, pp. C62–C63.

[2] S.-H. Lee et al., "A 5-Gb/s 0.25-μm CMOS jitter-tolerant variable-interval oversampling clock/data recovery circuit," IEEE J. Solid-State Circuits, vol. 37, no. 12, pp. 1822–1830, Dec. 2002.

[3] V. Stojanovic et al., "Autonomous dual-mode (PAM2/4) serial link transceiver with adaptive equalization and data recovery," IEEE J. Solid-State Circuits, vol. 40, no. 4, pp. 1012–1026, Apr. 2005.

[4] J. Park and P. P. Mercier, "A Sub-10-pJ/bit 5-Mb/s Magnetic Human Body Communication Transceiver," IEEE J. Solid-State Circuits, vol. 54, no. 11, pp. 3031-3042, Nov. 2019.

[5] W. Saadeh, M. A. B. Altaf, H. Alsuradi, and J. Yoo, "A 1.1-mW ground effect-resilient body-coupled communication transceiver with pseudo OFDM for head and body area network," IEEE J. Solid-State Circuits, vol. 52, no. 10, pp. 2690–2702, Oct. 2017.

[6] J. Zhao et al., "A 4-Mbps 41-pJ/bit on-off keying transceiver for body-channel communication with enhanced auto loss compensation technique," in Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC), Macau, Macao, Nov. 2019, pp. 173–176.

[7] Y. Jeon et al., "A 100Mb/s Galvanically-Coupled Body-Channel-Communication Transceiver with 4.75pJ/b TX and 26.8 pJ/b RX for Bionic Arms," 2019 Symposium on VLSI Circuits, 2019, pp. C292-C293, doi: 10.23919/VLSIC.2019.8778040.