Review on Resistive Termination Techniques Driven by Wireline Channel Behaviors

CHANGJAE MOON[1] **(Graduate Student Member, IEEE), MINSOO CHOI**[2] **(Member, IEEE),**
MYUNGGUK LEE[3]**, AND BYUNGSUB KIM**[1,4,5,6] **(Senior Member, IEEE)**

[1]Department of Electrical Engineering, Pohang University of Science and Technology, Pohang 37673, South Korea
[2]Department of Optical PHY Team, Marvell Technology, Santa Clara, CA 95054, USA
[3] Department of Standard HBM Group, Samsung Electronics, Hwaseong 18448, South Korea
[4]Department of Convergence IT Engineering, Pohang University of Science and Technology, Pohang 37673, South Korea
[5]Department of Semiconductor Engineering, Pohang University of Science and Technology, Pohang 37673, South Korea
[6]Institute for Convergence Research and Education in Advanced Technology, Yonsei University, Seoul 03722, South Korea

CORRESPONDING AUTHOR: B. KIM (e-mail: byungsub@postech.ac.kr)

ABSTRACT From the perspective of channel behaviors, we review several design techniques of resistive termination for wireline applications. Termination impedances strongly affect the channel behaviors. Their impacts vary a lot depending on the types of interconnects and the circuits. Therefore, termination impedances must be appropriately designed for the target applications. In this article, first, we explain an intuitive analytical transfer function model of wireline channels. The model allows designers to easily and intuitively understand the impacts of the termination resistances on the channel behaviors. Second, we review various resistive termination techniques for LC-dominant channels and discuss their design tradeoffs. Especially, we theoretically explain the relaxed impedance matching technique, which allows designers to violate impedance matching for design improvements at the cost of a negligible penalty in signal integrity. Third, we review various resistive termination techniques for RC-dominant channels and their design tradeoffs. We especially emphasize and theoretically explain why and how the design tradeoffs by resistive terminations in RC-dominant channels are different from the ones in LC-dominant channels.

INDEX TERMS Channel model, LC-dominant channels, RC-dominant channels, relaxed impedance matching, resistive termination.

I. INTRODUCTION

RESISTIVE termination with 50-Ω resistors is a trivial impedance matching method widely used in conventional standard 50-Ω applications. However, the simple 50-Ω matching too strictly constrains the transceiver (TRX) design, preventing design improvement beyond the 50-Ω matching constraint. Because the design challenges have been significantly increased after decades of advancements in wireline technology, the potential room for further improvement beyond the traditional 50-Ω matching constraint is increasingly attractive.

In LC-dominant applications, by carefully changing the channel behavior, the nonconventional design choice of resistive termination improves the link performance, such as eye height or power efficiency beyond the impedance matching constraint.

In emerging short-reach applications, such as interposers, chiplet, high bandwidth memory (HBM), and on-chip wires, the interconnects are expected to be scaled further toward RC-dominant interconnects in order to achieve higher data rate density and better energy efficiency. Because the characteristic impedance of an RC-dominant channel changes with
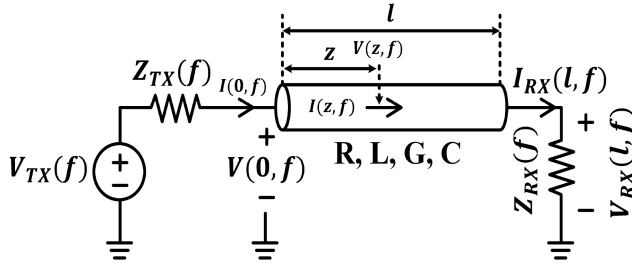
FIGURE 1. Schematic of a wireline channel model.

frequency and does not look resistive, resistive termination is no longer trivial at all. Therefore, in order to achieve the benefit of interconnect scaling, a designer must understand how to take advantages of the unique behavior of an RC-dominant channel in resistive termination design.

We review several design techniques of resistive termination from the perspectives of channel behaviors. In Section II, we explain an intuitive analytical channel model that provides design intuition on how resistive termination affects channel behaviors. In Sections III and IV, we review the characteristics of LC-dominant and RC-dominant channels as well as several design techniques for resistive termination driven by their channel behaviors, respectively.

II. INTUITIVE ANALYTICAL CHANNEL MODEL
In this section, we explain an intuitive analytical channel model in the frequency domain that helps designers easily understand various tradeoffs by resistive termination so that the designer can appropriately design the resistive termination considering the channel behavior and the overall link performance.

A. APPROXIMATE TRANSFER FUNCTION MODEL
A wireline channel is typically modeled as a transmission line (TL) having a transmitter (TX) and a receiver (RX) (Fig. 1). The TX is modeled as a Thévenin-equivalent circuit having a voltage source $V_{TX}(f)$ and an impedance $Z_{TX}(f)$. The RX is modeled as an input impedance $Z_{RX}(f)$. The interconnect of length l is modeled with RLGC parameters, where R, L, G, and C denote the per-unit-length resistance, inductance, conductance, and capacitance, respectively. $V(z, f)$ and $I(z, f)$ are the voltage and the current along the channel at a distance z from the TX, respectively (Fig. 1).

The channel's rigorous transfer function (4) can be derived by solving the telegrapher's equation (1), with boundary conditions (2) and (3) [1]

$$-\frac{\partial}{\partial z}\begin{bmatrix} V(z,f) \\ I(z,f) \end{bmatrix} = \begin{bmatrix} 0 & R+j2\pi fL \\ G+j2\pi fC & 0 \end{bmatrix}\begin{bmatrix} V(z,f) \\ I(z,f) \end{bmatrix} \quad (1)$$

$$V_{TX}(f) = V(0, f) + I(0, f)Z_{TX}(f) \quad (2)$$

$$V_{RX}(l, f) = I_{RX}(l, f)Z_{Rx}(f) \quad (3)$$

$$\frac{V_{RX}(l,f)}{V_{TX}(f)} = Z_C(f)Z_{RX}(f) / \left[\left(Z_C(f)^2 + Z_{TX}(f)Z_{RX}(f) \right) \sinh(\gamma(f)l) \right.$$
$$\left. + (Z_C(f)Z_{TX}(f) + Z_C(f)Z_{RX}(f)) \cosh(\gamma(f)l) \right] \quad (4)$$

where $Z_C(f)$ and $\gamma(f)$ are the characteristic impedance and propagation constant of the interconnect, respectively

$$Z_C(f) = \sqrt{\frac{(R+j2\pi fL)}{(G+j2\pi fC)}} \quad (5)$$

$$\gamma(f) = \sqrt{(R+j2\pi fL)(G+j2\pi fC)}. \quad (6)$$

Although (4) is rigorously derived without approximation, it is too complex to provide design intuition. Instead, (4) can be rewritten into the same but more intuitive formula

$$\frac{V_{RX}(l,f)}{V_{TX}(f)} = \frac{Z_C(f)}{Z_{TX}(f)+Z_C(f)}2e^{-l\gamma(f)}\frac{Z_{RX}(f)}{Z_C(f)+Z_{RX}(f)}\frac{1}{1-\eta(f)} \quad (7)$$

where $\eta(f) = \Gamma_{TX}(f)\Gamma_{RX}(f)e^{-2l\gamma(f)}$, $\Gamma_{TX}(f) = (Z_{TX}(f) - Z_C(f))/(Z_{TX}(f) + Z_C(f))$, and $\Gamma_{RX}(f) = (Z_{RX}(f) - Z_C(f))/(Z_{RX}(f)+Z_C(f))$. $\Gamma_{TX}(f)$ and $\Gamma_{RX}(f)$ are the reflection coefficients at the TX and the RX, respectively. $\eta(f)$ is the round-trip gain of a reflected wave traveling back and forth between the TX and the RX.

The term $1/(1 - \eta(f))$ in (7) complicates the channel behavior if $\eta(f) \neq 0$. A complex channel behavior is not preferred in wireline applications because it requires complex hardware to implement broadband signaling. For this reason, resistive terminations are usually designed to simplify the channel behavior for a broad frequency range. Because $|\eta(f)|$ is the product of three terms $|\Gamma_{TX}(f)|$, $|\Gamma_{RX}(f)|$, and $|e^{-2l\gamma(f)}|$, all of which are usually smaller than 1, designers can easily make $|\eta(f)| \ll 1$ in most practical designs, where reflection is avoided. For instance, if $|\Gamma_{TX}(f)| = 0.5$, $|\Gamma_{RX}(f)| = 0.5$, and $|e^{-2l\gamma(f)}| = 0.5$, then $|\eta(f)| = 0.0625 \ll 1$ even though the reflection coefficients are large: this condition ($|\eta(f)| \ll 1$) is traditionally enforced by impedance matching ($|\Gamma_{TX}(f)| = |\Gamma_{RX}(f)| = 0$). Therefore, we may assume (8), and approximate (7)–(9), an intuitive closed-form transfer function of a wireline channel

$$|\eta(f)| = |\Gamma_{TX}(f)\Gamma_{RX}(f)e^{-2l\gamma(f)}| \ll 1 \quad (8)$$

$$\frac{V_{RX}(l,f)}{V_{TX}(f)} \approx \frac{Z_C(f)}{Z_{TX}(f)+Z_C(f)}2e^{-l\gamma(f)}\frac{Z_{RX}(f)}{Z_C(f)+Z_{RX}(f)}. \quad (9)$$

Equation (9) accurately describes the transfer function if the validity condition (8) is satisfied [2].

The approximate transfer function (9) can be intuitively modeled using an equivalent voltage-controlled voltage source (VCVS) model of a TL (Fig. 2). The circuit model of the channel in Fig. 2(a) is obtained by replacing the TL in Fig. 1 with the equivalent VCVS model, which has input and output impedances of $Z_c(f)$ and a gain of $2e^{-l\gamma(f)}$. $Z_c(f)$ is the characteristic impedance (5), and the channel's length l is included in the VCVS gain $2e^{-l\gamma(f)}$.

If the current-mode TX or the current-model RX is used, the model can be easily modified. The current-mode TX can be modeled with a Norton-equivalent current source $I_{TX}(f)$ with an impedance $Z_{TX}(f)$ [Fig. 2(b)] instead of a Thévenin-equivalent circuit of the voltage-mode TX in Fig. 2(a). If the current-mode RX is used instead of the voltage-mode RX,
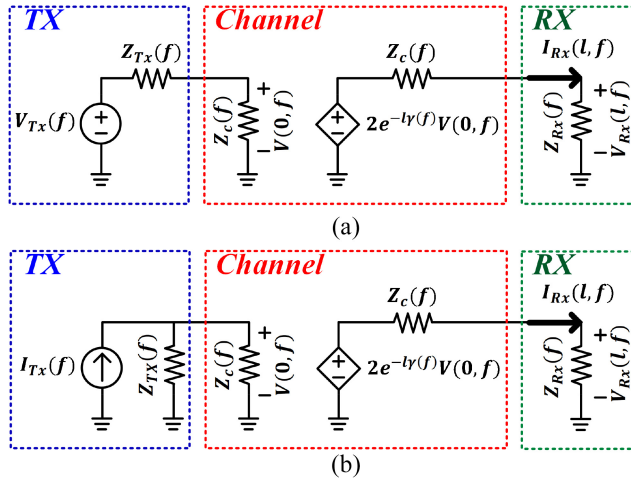
FIGURE 2. Intuitive circuit models of wireline channels having (a) voltage-mode and (b) current-mode TXs with RXs.

the input current into the same RX impedance $Z_{RX}(f)$ can be used as the received signal instead of the voltage across $Z_{RX}(f)$ (Fig. 2).

The transfer function $V_{RX}(l,f)/I_{TX}(f)$ of the channel with a current-mode TX and a voltage-mode RX is

$$\frac{V_{RX}(l,f)}{I_{TX}(f)} \approx \frac{Z_{TX}(f)Z_C(f)}{Z_{TX}(f) + Z_C(f)} 2e^{-l\gamma(f)} \frac{Z_{RX}(f)}{Z_C(f) + Z_{RX}(f)}. \quad (10)$$

With a voltage-mode TX and a current-mode RX, the transfer function $I_{RX}(l,f)/V_{TX}(f)$ is

$$\frac{I_{RX}(l,f)}{V_{TX}(f)} \approx \frac{Z_C(f)}{Z_{TX}(f) + Z_C(f)} 2e^{-l\gamma(f)} \frac{1}{Z_C(f) + Z_{RX}(f)}. \quad (11)$$

With a current-mode TX and a current-mode RX, the transfer function $I_{RX}(l,f)/I_{TX}(f)$ is

$$\frac{I_{RX}(l,f)}{I_{TX}(f)} \approx \frac{Z_{TX}(f)Z_C(f)}{Z_{TX}(f) + Z_C(f)} 2e^{-l\gamma(f)} \frac{1}{Z_C(f) + Z_{RX}(f)}. \quad (12)$$

The transfer functions (9)–(12) can be easily extended even if the TX and the RX impedances are not resistive and have extra parasitic components [2]. Equations (9)–(12) hold even though the TX and RX impedances are not resistive. If there are parasitic capacitors or inductors at the TX and RX, then the parasitic elements can be added to the circuit model (Fig. 2) while the validity condition (8) must be appropriately modified by using Thévenin's and Norton's theorems [2].

B. DESIGN INTUITION FOR TERMINATION IMPEDANCES

The channel models provide two simple, intuitive, separate formulas to understand how the TX and the RX impedance affect the channel behavior. In (9), the transfer function can be interpreted as a product of the three terms: 1) the voltage division between the TX impedance and the channel's characteristic impedance $Z_C(f)/(Z_{TX}(f) + Z_C(f))$; 2) the interconnect's attenuation ($2e^{-l\gamma(f)}$) modeled by a VCVS; and 3) the voltage division between the channel's characteristic impedance and the RX impedance $Z_{RX}(f)/(Z_C(f) +$

$Z_{RX}(f))$ (Fig. 2). Because this transfer function model has three separate terms for the TX, the interconnect, and the RX, this formula provides a clear intuition of how each of these components affects the channel behavior. The impedance $Z_{TX}(f)$ of the TX appears only in the first voltage division term at the TX, whereas the RX impedance $Z_{RX}(f)$ appears only in the third voltage division term at the RX. The length l of the interconnect and the propagation constant $\gamma(f)$ only appear in the second interconnect's attenuation term. Therefore, during the TX impedance design, a designer can only focus on the $Z_C(f)/(Z_{TX}(f) + Z_C(f))$ term in order to consider the channel behavior affected by the $Z_{TX}(f)$ without considering the other two terms that are independent of $Z_C(f)$. Similarly, when designing the RX impedance, the designer can only focus on the $Z_{RX}(f)/(Z_C(f) + Z_{RX}(f))$ term without considering the other two terms. Therefore, if the validity condition (8) is satisfied, we can interpret these terms as the interconnect-TX and interconnect-RX interaction terms, respectively. A similar discussion holds for the other three transfer function cases (10)–(12).

III. RESISTIVE TERMINATION TECHNIQUES FOR _LC_-DOMINANT CHANNELS

In this section, we review several resistive termination techniques from the perspective of LC-dominant channel behaviors in the frequency domain. First, we explain the characteristics of an LC-dominant channel using the intuitive model explained in Section II, and then we review several resistive termination techniques, especially, emphasizing the relaxed impedance matching technique that enables a design beyond the limitation of the impedance matching constraint.

A. CHARACTERISTICS OF LC-DOMINANT CHANNELS

Typical interconnects are LC-dominant channels. Ideally, they do not suffer from channel losses because the resistance R and conductance G parameters are negligible in their ideal RLGC model. However, in reality, skin effect and dielectric loss cause significant channel loss.

Skin effect is a phenomenon that the current concentrates on the conductor's surface at high frequencies because of the induced magnetic field in the conductor. This effect slows phase velocity and increases series impedance and attenuation. Skin depth δ_s is the distance where current density decreases by e^{-1} and can be expressed as

$$\delta_s = \sqrt{\frac{\rho}{\pi f \mu}} \quad (13)$$

where ρ, μ, and f are the electrical resistivity, permeability, and the frequency, respectively [3], [4], [5]. The surface impedance Z_s is given by

$$Z_s = \sqrt{\pi f \mu \rho}(1 + j) = R_s\sqrt{f}(1 + j) \quad (14)$$

where $R_s = \sqrt{\pi \mu \rho}$ is the skin effect parameter [4], [5].

Dielectric loss refers to the energy dissipation within the dielectric material of the TLs. This loss is primarily
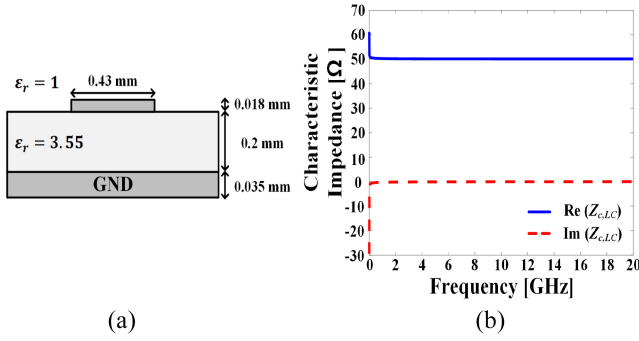
FIGURE 3. (a) Cross-sectional view of an example LC-dominant interconnect. (b) Simulated characteristic impedance of the LC-dominant interconnect versus the frequency.
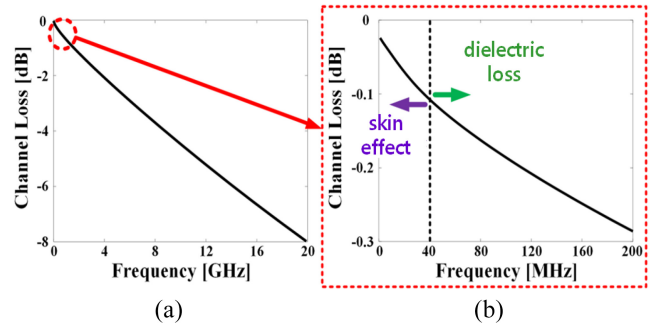

FIGURE 4. (a) The simulated LC-dominant channel loss versus the frequency when the channel length is 10 cm. (b) Dominant sources of the loss identified in the channel loss plot of Figure 4(a).

characterized by the loss tangent $\tan \delta_d$, which is a ratio of the material's energy loss to the energy stored within it. The loss tangent is the ratio of the imaginary part to the real part of the dielectric constant [3], [4]. Materials with higher loss tangents will experience greater dielectric losses, leading to increased signal attenuation and reduced transmission efficiency. The dielectric loss parameter G_d is given by

$$G_d = 2\pi C \tan \delta_d \tag{15}$$

where C is the per-unit-length capacitance [3].

To model the skin effect and dielectric loss, $R + j2\pi fL$ and $G + j2\pi fC$ terms in (1) are modified as

$$R + j2\pi fL = R_0 + R_s\sqrt{f} + j\left(2\pi fL + R_s\sqrt{f}\right) \tag{16}$$

$$G + j2\pi fC = G_0 + fG_d + j2\pi fC. \tag{17}$$

R_0 and G_0 are the static resistance and the conductance parameters, respectively.

In LC-dominant channels, the inductance L and capacitance C parameters are dominant in the TL while R_0 and G_0 are negligible [6]

$$2\pi fL \gg R_s\sqrt{f} \gg R_0, \quad 2\pi fC \gg G_d f \gg G_0. \tag{18}$$

With conditions (18), (16) can be simplified to

$$R + j2\pi fL \approx R_0 + R_s\sqrt{f} + j2\pi fL. \tag{19}$$

With (18) and (19), the characteristic impedance (20) and propagation constant (21) of an LC-dominant channel can be derived [6]

$$Z_{C,\text{LC}}(f) \approx Z_0 = \sqrt{L/C} \tag{20}$$

$$\gamma_{\text{LC}}(f) \approx j2\pi\sqrt{LC}f + \frac{R_s}{2Z_{C,\text{LC}}}\sqrt{f} + \frac{G_d Z_{C,\text{LC}}}{2}f. \tag{21}$$

Even with skin effect and dielectric loss, the characteristic impedance $Z_{C,\text{LC}}(f)$ of an LC-dominant interconnect is almost the same constant resistance as the characteristic impedance $Z_0 = \sqrt{L/C}$ of the ideal TL (20). In a 2-D field solver simulation of an example LC-dominant microstrip line [Fig. 3(a)], $Z_{C,\text{LC}}(f) \approx 50$ Ω across a very wide frequency range [Fig. 3(b)]. Therefore, even with skin effect

and dielectric loss, a typical LC-dominant interconnect with $Z_{C,\text{LC}}(f) \approx 50$ Ω can be resistively terminated with 50-Ω resistors like an ideal 50-Ω TL.

Although skin effect and dielectric loss barely change $Z_{C,\text{LC}}(f)$, they greatly increase the channel loss. By substituting (20) and (21) into (9), we can approximate the transfer function $V_{\text{RX}}(l,f)/V_{\text{TX}}(f)$ of an LC-dominant channel with skin effect and dielectric loss

$$\frac{V_{\text{RX}}(l,f)}{V_{\text{TX}}(f)} \approx \frac{Z_0}{Z_{\text{TX}}(f) + Z_0} 2e^{-l\left(j2\pi\sqrt{\text{LC}}\right)f} \frac{Z_{\text{RX}}(f)}{Z_0 + Z_{\text{RX}}(f)}$$
$$\times e^{-l\left(\frac{R_s}{2Z_0}\right)\sqrt{f}} e^{-l\left(\frac{G_d Z_0}{2}\right)f}$$
$$= \text{TF}_{\text{wo}}(f) \times e^{-l\left(\frac{R_s}{2Z_0}\right)\sqrt{f}} e^{-l\left(\frac{G_d Z_0}{2}\right)f} \tag{22}$$

where $\text{TF}_{\text{wo}}(f)$ is the transfer function of an LC-dominant channel without skin effect and dielectric loss. It is noticeable that the channel loss contribution $e^{-l(R_s/2Z_0)\sqrt{f}}$ by the skin effect as well as the channel loss contribution $e^{-l(G_d Z_0/2)f}$ by the dielectric loss are multiplied to the transfer function $\text{TF}_{\text{wo}}(f)$ in (22). In a typical LC-dominant channel, the first skin-effect term is approximately proportional to the length l and $\sqrt{f}$ while the second dielectric-loss term is roughly proportional to both l and f. In the simulation of an example LC-dominant channel, the loss-versus-frequency plot has a square-root curvature at low frequencies (< 40 MHz) because the skin effect primarily contributes to the channel loss. On the other hand, the plot is linear at high frequencies (> 40 MHz) because the dielectric loss becomes dominant (Fig. 4). The loss is usually compensated by equalization in a conventional link design.

It is noticeable that the condition (18) for an LC-dominant channel depends on various factors: dimensions and materials of interconnects as well as operation frequencies. As long as (18) is satisfied, cables, micro-strip lines, or strip lines can be considered as LC-dominant channels. Typically, most large-scale interconnects, such as cables, backplane traces, PCB traces, and package interconnects, can be considered as LC-dominant channels. However, depending on the widths and spaces of lines as well as operating frequency, scaled interconnects, such as interposer and on-chip wires, can be also LC-dominant channels, too.
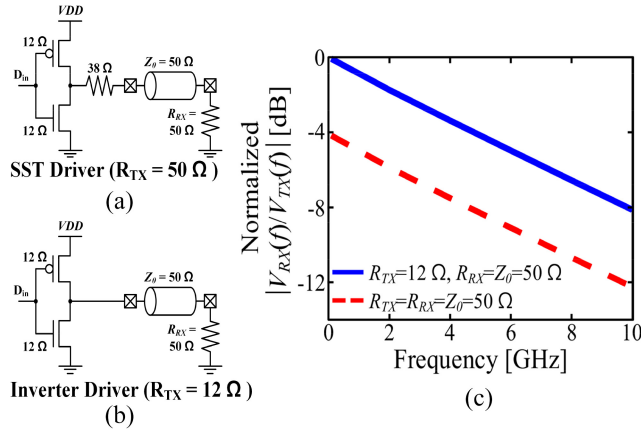
FIGURE 5. Schematic of (a) SST driver and (b) inverter driver. (c) Simulated transfer function $|V_{RX}(l,f)/V_{TX}(f)|$ values of TRXs with conventional impedance matching ($R_{TX} = R_{RX} = Z_0 = 50$ Ω) and with relaxed impedance matching ($R_{TX} = 12$ Ω, $R_{RX} = Z_0 = 50$ Ω) [14].
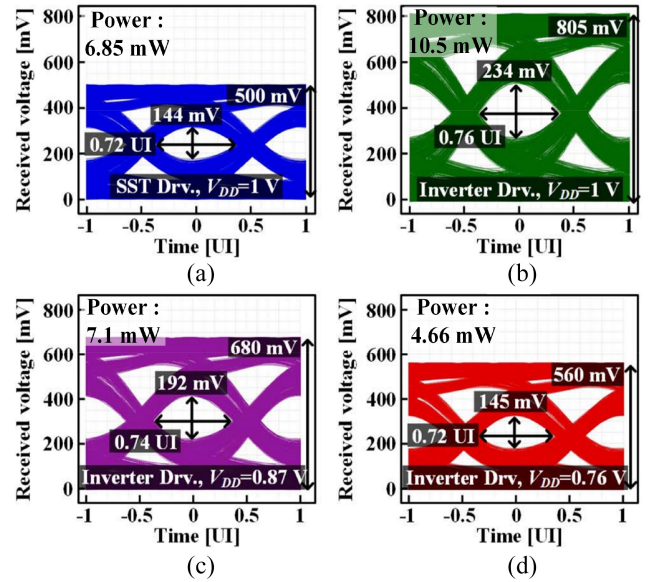

FIGURE 6. Simulated 20-Gb/s eye diagrams measured at the far-end of the channel (a) when an SST driver operates with 1-V supply voltage, and when an inverter driver operates with supply voltages of (b) 1 V, (c) 0.87 V, and (d) 0.76 V, respectively [14]. The same inverter driver was used in (b)–(d). In (c) and (d), the supply voltage was reduced to achieve about the same power and the same eye height of the SST driver in (a).

B. CONVENTIONAL IMPEDANCE MATCHING TECHNIQUE

Impedance matching is the most popular and conservative termination technique in order to ensure signal integrity [7], [8], [9], [10], [11]. In this technique, the TX and the RX are terminated using resistors with the characteristic impedance of the channel: $Z_{TX}(f) = R_{TX} = Z_0$; $Z_{RX}(f) = R_{RX} = Z_0$; $Z_{C,LC}(f) = Z_0$. Because the characteristic impedance of an LC-dominant channel is approximately a constant resistance in a wide frequency range as expressed in (20), it theoretically ensures "zero" signal reflection: $\Gamma_{TX}(f) = 0$ and $\Gamma_{RX}(f)=0$. As a result, the validity condition (8) is satisfied ($|\Gamma_{TX}(f)\Gamma_{RX}(f)e^{-2l\gamma(f)}| = 0 \ll 1$), and a simple transfer function (23) can be theoretically derived from (9) as

$$\frac{V_{RX}(l,f)}{V_{TX}(f)} = \frac{1}{2}e^{-l\gamma(f)} \tag{23}$$

where $\gamma(f) = \gamma_{LC}(f)$ as in (9). Therefore, in order to provide the best signal integrity by making the theoretical channel behavior as simple as possible, designers widely use this technique in a wide range of applications from 224-Gb/s long-reach differential wireline transceivers [7], [8] to short-reach single-ended on-/off-package links for 20–40-Gb/s data rates [9], [10], [11].

C. RELAXED IMPEDANCE MATCHING TECHNIQUE

Relaxed impedance matching is a method that deliberately creates small mismatches in termination impedances to enhance the performance of high-speed TRXs in various aspects [12], [13], [14], [15], [16], [17], [18], [19]. We will explain the relaxed impedance matching in comparison with the impedance matching.

In the traditional impedance matching design, it is noticeable that the spectral shape is solely determined by the propagation constant $\gamma(f)$ because the other terms are not functions of f in (23).

If R_{TX} and R_{RX} (not necessarily equal to Z_0) satisfy the validity condition (8), then the transfer function (9) becomes

$$\frac{V_{RX}(l,f)}{V_{TX}(f)} \approx \frac{Z_0}{R_{TX} + Z_0} 2e^{-l\gamma(f)} \frac{R_{RX}}{Z_0 + R_{RX}}. \tag{24}$$

Because $\gamma(f) = \gamma_{LC}(f)$ is the only frequency-dependent term in (24) as in impedance matching case (23), the transfer functions (23) and (24) have identical spectral shapes and differ only in magnitude. As a result, as long as R_{TX} and R_{RX} satisfy (8), the signal integrity penalty is negligible. This constraint (8) is more relaxed than impedance matching, and therefore, it is called "relaxed impedance matching" [13]. The design space set by the relaxed impedance matching constraint (8) is larger than one set by impedance matching. Therefore, the link design can be improved with relaxed impedance matching.

By reviewing several design examples, we will explain how the relaxed impedance matching technique can improve the link design.

1) SINGLE-SIDED TERMINATION TECHNIQUE

The single-sided termination technique is a design technique in which only one side of a link is terminated with a characteristic impedance of the interconnect while the other side is not matched [14], [15], [16], [17], [18], [19]. Because either $\Gamma_{TX}(f) = 0$ or $\Gamma_{RX}(f) = 0$, the relaxed impedance matching condition is satisfied as $|\Gamma_{TX}(f)\Gamma_{RX}(f)e^{-2l\gamma(f)}| = 0 \ll 1$. Therefore, the single-sided termination can be considered as a more strict practice of relaxed impedance matching.

The single-sided termination technique can increase the voltage swing of short-reach interfaces. Lee et al. [14] proposed a short-reach link with a 20-Gb/s/ch inverter TX
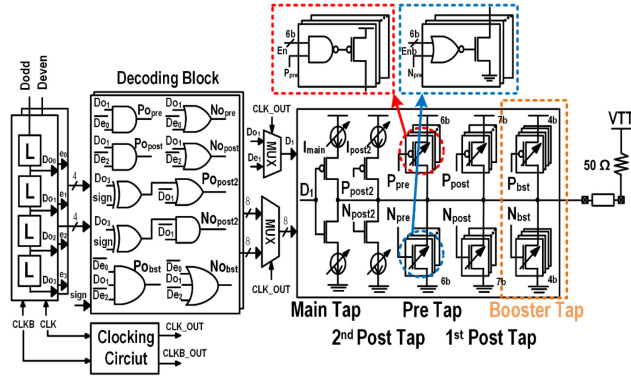
FIGURE 7. Schematic of the implemented 4-tap addition-only FFE (A-FFE) TX using far-end matching [16].

TABLE 1. Energy efficiencies of an inverter driver and an SST driver for the same eye-opening [14].

	Inverter [Fig. 6(d)]	SST [Fig. 6(a)]
Terminated Resistance [Ω]	24	50
Power Supply [V]	0.76	1
Data Rate [Gb/s]	20	20
Eye Height [mV]	145	144
Energy Efficiency [pJ/b]	0.233	0.343

that has an impedance ($R_{TX} = 12$ Ω) smaller than the characteristic impedance of the interconnect ($Z_0 = 50$ Ω) and the impedance-matched RX ($R_{RX} = Z_0$) [Fig. 5(b)]. Because $\Gamma_{RX}(f) = 0$, (8) is satisfied, and thus the transfer function is approximately

$$\frac{V_{RX}(l,f)}{V_{TX}(f)} = \frac{Z_0}{R_{TX} + Z_0} e^{-l\gamma(f)}. \qquad (25)$$

Because $R_{TX} < Z_0$, the magnitude of the transfer function (25) is increased by $Z_0/(R_{TX}+Z_0)$ times (about 4.15 dB) [Fig. 5(c)] compared with the one with the conventional impedance matching (23) implemented by a source-series termination (SST) driver [Fig. 5(a)]. Therefore, the eye-opening is also improved by 62% [Fig. 6(a) and (b)] consuming 43% more power due to the increased swing.

The swing improvement can be traded for power efficiency by reducing the supply voltage. With the reduced supply voltage (0.87 V) for the same power consumption, the inverter TX has a 33% larger eye size than its SST counterpart [Fig. 6(c)]. At further reduced supply voltage (0.76 V), the inverter TX consumes 30% less power than the SST TX for the same eye-opening by trading the swing improvement for power efficiency [Fig. 6(d)]. The TX area is also reduced by about 76% by removing the 38-Ω series resistor for matching [14]. Table 1 compares the metrics of the SST driver [Fig. 6(a)] and the inverter driver [Fig. 6(d)].
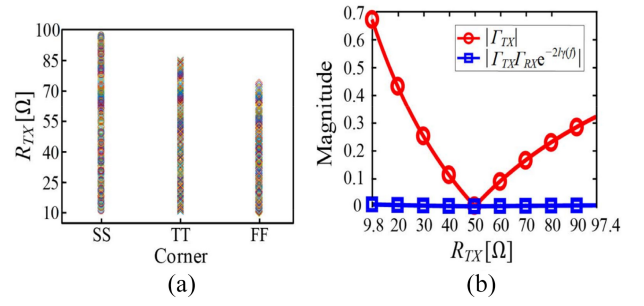

FIGURE 8. (a) Simulated R_{TX} ranges at SS, TT, and FF corners for an inverter-based driver with input/output voltages swept from 0 to 1.1 V, and (b) simulated $|\Gamma_{TX}|$ values and validity condition for the estimated R_{TX} range [14].
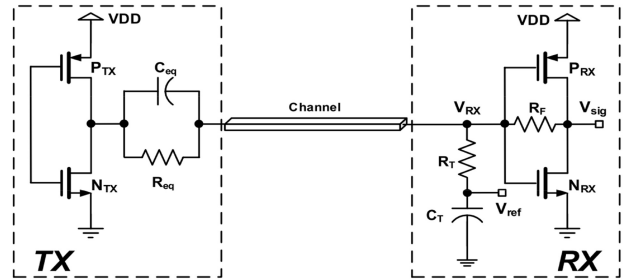

FIGURE 9. Single-side terminated TRX with high-impedance TX and impedance-matched RX [17].

The single-sided termination technique also enables the inverter-based feedforward equalization (FFE) TX to overcome the channel loss. Moon et al. proposed a 20-Gb/s/ch inverter-based FFE TX with the RX matching [15], [16] (Fig. 7). Although the TX impedance fluctuates due to switching of inverter-based FFE taps and the nonlinearity of the inverter, the validity condition (8) can be satisfied due to the RX matching ($\Gamma_{RX}(f) = 0$). Because the condition (8) can be satisfied due to the RX termination even if the inverter's output impedance varies from 9.8 to 97.4 Ω, the channel's spectral shape is preserved (Fig. 8) [14]. The nonlinearity of the inverter can be compensated by predistorting FFE coefficient [24], [25]. Therefore, the linear FFE can be implemented using the inverter drivers [15], [16] to improve the output swing by 74%.

Similarly, a 20-Gb/s compact equalization utilizing capacitive peaking can be implemented at the TX side with only RX-side matching (Fig. 9) [17]. In this approach, the TX matching is violated by the resistor and the capacitor, while the RX impedance matching is provided by the transimpedance amplifier (TIA) (Fig. 9).

Also, Jin et al. used the single-side impedance matching with 1-tap fractional spaced feedforward equalization (FS-FFE) to improve the signal-to-noise ratio (SNR) in a four-level pulse-amplitude modulation (PAM4) signal [18], [19]. The termination resistances are optimized as $R_{TX} = 20$ Ω and $R_{RX} = 50$ Ω for optimal balancing between power and area (Fig. 10). In particular, using a tap spacing of 0.8 unit interval (UI), this termination design achieved $2.25\times$ improvement in eye opening compared to $R_{TX} =$
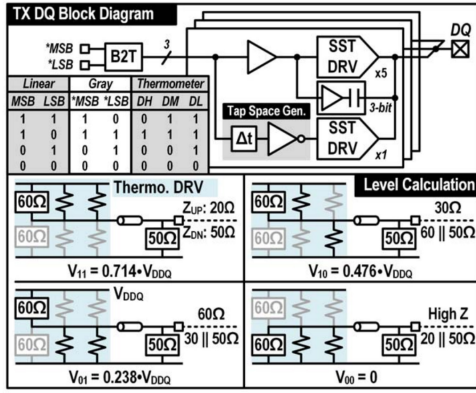
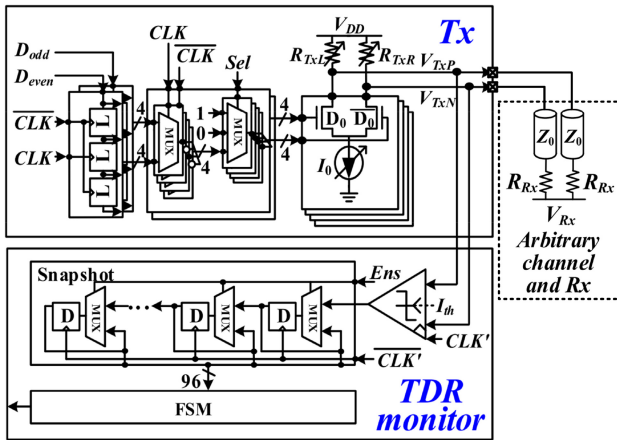**FIGURE 10.** PAM4 TX block diagram with single-sided matching [18].

FIGURE 11. 4-tap FFE TX, which automatically and adaptively relaxed impedance matching, using an on-chip time-domain reflectometer monitor [13].
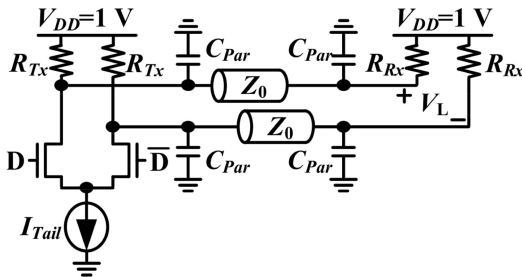

FIGURE 12. Example of an interconnect with a CML TX and a voltage-mode RX. Parasitic capacitors C_{par} are present at the TX output and RX input [13].

$R_{RX} = 50$ Ω at the data rate of 16 Gb/s/ch, demonstrating the effectiveness of the single-sided termination.

2) ADAPTIVE RELAXED IMPEDANCE MATCHING FOR ARBITRARY IMPEDANCE COMPATIBILITY

Choi et al. proposed an adaptive relaxed impedance matching technique to automatically adjust the TX impedance to maximize eye opening for arbitrary characteristic impedances Z_0 of the interconnect and the RX impedance R_{RX} (Fig. 11) [12], [13]. A 12-Gb/s current mode logic (CML) style FFE TX was designed (Fig. 12), and thus the TX
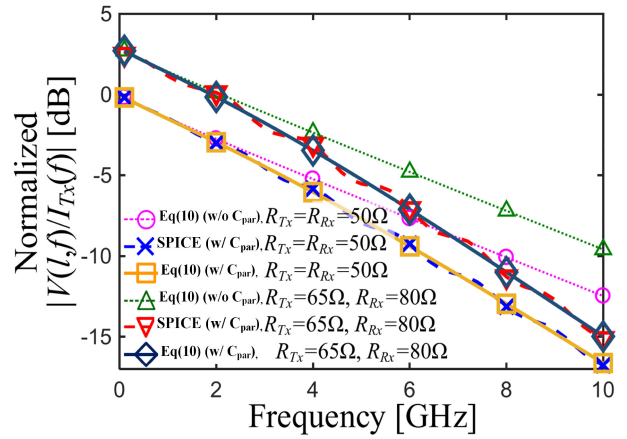

FIGURE 13. Magnitude of transfer function $|V_{RX}(l, f)/I_{TX}(f)|$ of the interconnect (Fig. 11) with various $Z_0 = 50$ Ω, $C_{par} = 500$ fF, and various R_{TX} and R_{RX} configuration [13].
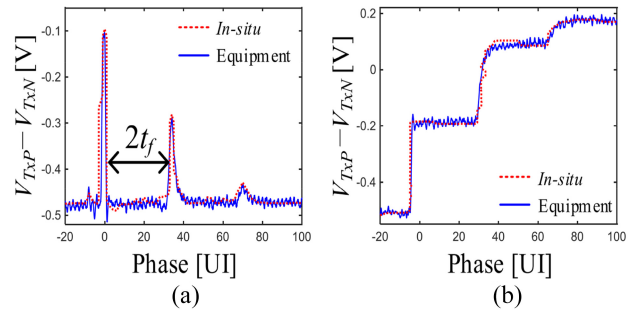

FIGURE 14. TX output voltages measured by the TDR monitor and by equipment at 8 Gb/s while transmitting (a) square pulse and (b) step with $Z_0 = 35$ Ω and $R_{RX} = 200$ Ω [13].

impedance larger than 50 Ω can improve the signal amplitude. Even with parasitic capacitances of 500 fF at both ends, an example relaxed impedance matching configuration of the TRX ($R_{TX} = 65$ Ω, $R_{RX} = 80$ Ω) improves the swing with a slightly steeper channel roll-off (Fig. 13). R_{TX} can be automatically adjusted to maximize the eye opening for arbitrary R_{RX} and Z_0. The time-domain reflectometry (TDR) monitor attached at the TX output node detects R_{RX} and Z_0 by monitoring a single-bit pulse response and a step response (Fig. 14). The TX achieved high-quality eye opening for arbitrary Z_0 ranging 35–75 Ω and R_{RX} ranging 30–200 Ω, enabling seamless compatibility between various impedance standards in wireline applications (Fig. 15) [12], [13]. Table 2 compares metrics of the conventional impedance matching and the adaptive relaxed impedance matching when $R_{RX} = Z_0 = 35$ Ω. For similar eye sizes, the relaxed impedance-matched CML TX requires only 84% of the total tap current and achieves 80% of the energy efficiency of the conventional impedance-matched TX.

D. IMPEDANCE MISMATCH WITH REFLECTION CANCELLATION

Lee et al. [20] proposed deliberately to use large termination resistances for a single-ended DRAM interface TRX in order
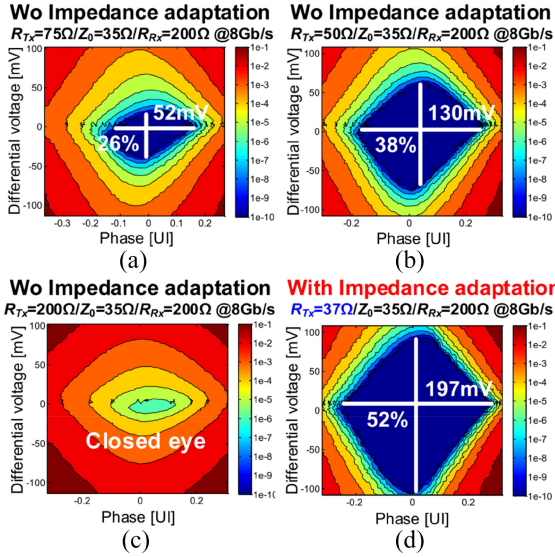
FIGURE 15. Eye diagrams were measured in-situ at the RX using four different TX configurations: (a) 75-Ω TX, (b) 50-Ω TX, (c) TX with $R_{TX} = R_{RX} = 200$ Ω, and (d) adaptive-impedance TX [13]. All TXs transmitted data at 8 Gb/s to a 200-Ω R_{RX} through a 35-Ω channel and utilized a 16.3-mA tap current [13].
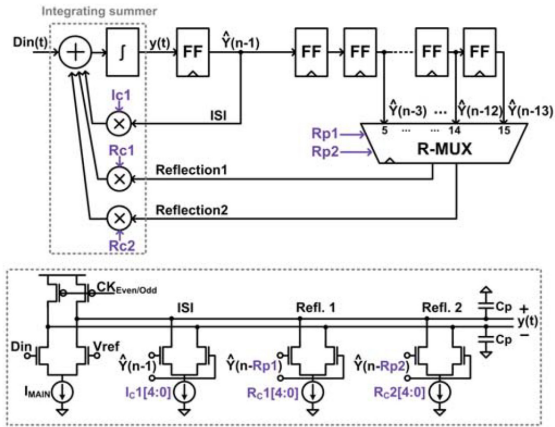

FIGURE 16. 3-tap integrating DFE and a half-rate current-integrating summer to cancel reflections and to compensate for ISI [20].

to reduce the TRX power consumption while canceling the reflections by decision feedback equalization (DFE). Typically, with conventional impedance matching ($R_{TX} = R_{RX} = Z_0$), signaling power is $VDD^2/(4Z_0)$. In [20], termination resistance is deliberately increased to $4Z_0$ in order to reduce the power to $VDD^2/(16Z_0)$. However, it increases both intersymbol interference (ISI) and reflection. These effects were compensated using an integrating DFE circuit at the RX, with two taps for reflection and one tap for ISI (Fig. 16). Increasing R_{TX} and R_{RX} from Z_0 to $4Z_0$ reduces the output driver power by 9.38 mW and increases the normal mode RX power by 4.1 mW at 5 Gb/s. This reduces the transceiver power by 5.28 mW, corresponding to a 26.7% reduction.

Similarly, for die-to-die (D2D) chiplet interface, Seong et al. [21] proposed a 32-Gb/s/ch TX with a reflection-cancellation driver (RCD) that compensates for the
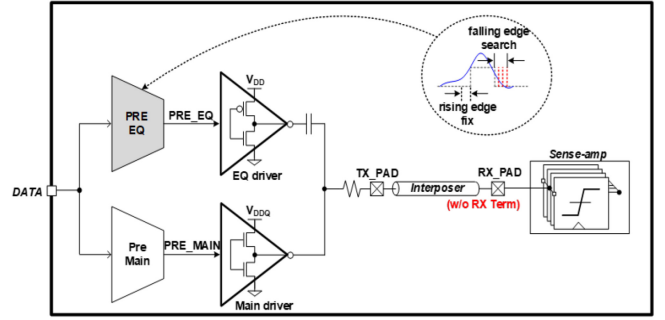

FIGURE 17. Reflection cancellation driver to eliminate the effect of the reflected signal from the RX pad [21].

TABLE 2. Energy efficiencies of CML TXs with conventional and relaxed impedance matching [13].

		Conventional Matching	Relaxed Impedance Matching
	TX Termination [Ω]	**35**	**131** (Automatically adapted)
	Tap Current [mA]	**20**	**16.8**
$Z_0 = 35$ Ω, $R_{RX} = 35$ Ω	**Data Rate [Gb/s]**	**12**	**12**
	Eye Height [mV]	**84.6**	**83.8**
	Eye Width [UI]	**0.528**	**0.516**
	Energy Efficiency [pJ/b]	**1.975**	**1.583**

reflections due to the impedance mismatch when the RX's on-die termination is not utilized (Fig. 17). A predriver in the RCD finds an optimal compensation setup to remove signal distortion caused by reflection.

IV. RESISTIVE TERMINATION TECHNIQUE FOR *RC*-DOMINANT CHANNELS

In this section, we explain the unique characteristics of RC-dominant channels in the frequency domain as well as why and how the design tradeoffs by resistive terminations in RC-dominant channels are different from the ones in LC-dominant channels with reviews of several design techniques.

A. CHARACTERISTICS OF RC-DOMINANT CHANNELS
In typical RC-dominant applications [Fig. 18(a)], fine-pitch interconnects are tightly packed in small areas in order to accommodate numerous connections between components in a limited space [27]. The high-density routing is important in die-to-die interfaces or intrachip interconnects where the power efficiency and the total throughput are important. Because wires are narrow and closed-spaced in such applications, the resistance R and capacitance C are dominant in the impedance Z and the admittance Y of the interconnect: $R \gg 2\pi f L$ and $2\pi f C \gg G$. Therefore, the characteristic impedance (26) and the propagation constant (27) can be derived from (5) and (6) as

$$Z_{C, \text{ RC}}(f) \approx \sqrt{R/j2\pi fC} \qquad (26)$$

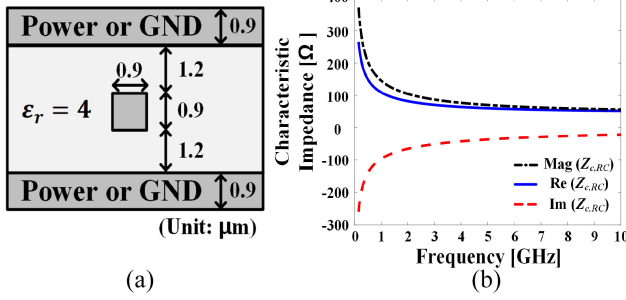$$\gamma_{\text{RC}}(f) \approx \sqrt{j2\pi f\text{RC}}. \qquad (27)$$

FIGURE 18. (a) Cross-sectional view of an example RC-dominant interconnect. (b) Simulated characteristic impedance of the RC-dominant interconnect versus the frequency.
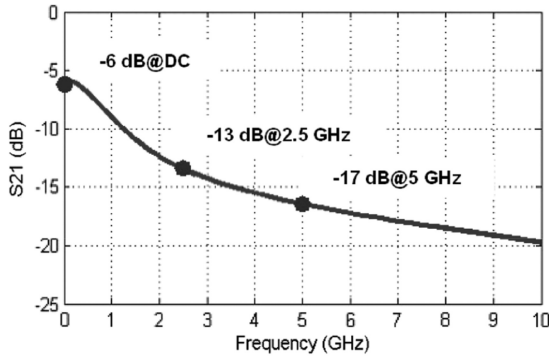

FIGURE 19. Simulated loss of a silicon carrier versus frequency. The channel length is 20 mm [23].

FIGURE 20. Interconnect-TX interaction terms of (a) voltage-mode TX, $(Z_{C,RC}(f)||Z_{par}(f))/(R_{TX} + Z_{C,RC}(f)||Z_{par}(f))$, and (b) current-mode TX, $R_{TX}[Z_{C,RC}(f)||Z_{par}(f)]/(R_{TX} + Z_{C,RC}(f)||Z_{par}(f))$. $Z_{par}(f)$ is the impedance of parasitic capacitance of $C_{par} = 100$ fF at the TX output node. The RLGC parameters used in the channel are $R = 53.419$ mΩ/μm, $L = 0.236$ pH/μm, $C = 0.198$ fF/m, and $G = 0$ mS/μm, respectively.

FIGURE 21. Interconnect-RX interaction terms of (a) voltage-mode RX, $(R_{RX}||Z_{par}(f))/(Z_{C,RC}(f) + R_{RX}||Z_{par}(f))$, and (b) current-mode RX, $Z_{par}(f)/\{(Z_{C,RC}(f) + R_{RX}||Z_{par}(f)) \times (R_{RX} + Z_{par}(f))\}$, where $Z_{par}(f)$ is the impedance of parasitic capacitance of $C_{par} = 100$ fF at the RX input node.

The validity condition (8) is usually satisfied by a significant attenuation of wire and the TX and RX reflection coefficients smaller than 1. Consequently, with the termination resistances R_{TX} and R_{RX} of the TX and the RX, we can express the transfer function $V_{RX}(l,f)/V_{TX}(f)$ using

$$\frac{V_{RX}(l,f)}{V_{TX}(f)} \approx \frac{Z_{C,\,RC}(f)}{R_{TX}(f) + Z_{C,\,RC}(f)} 2e^{-l\gamma_{RC}(f)} \frac{R_{RX}(f)}{Z_{C,RC}(f) + R_{RX}(f)}. \quad (28)$$

A typical RC-dominant channel has a frequency response proportional to $\sqrt{f}$ due to $\gamma_{RC}(f) \approx \sqrt{j2\pi f RC}$ (Fig. 19). The channel loss can be easily compensated by equalization techniques [22], [23], [24], [25].

In RC-dominant channels [Fig. 18(a)], the characteristic impedance $Z_{C,\,RC}(f)$ has a low-pass filter nature [Fig. 18(b)] unlike in LC-dominant channels, where $Z_{C,\,LC}(f) \approx Z_0$. As a result, the voltage division terms $Z_{C,RC}(f)/(R_{TX} + Z_{C,RC}(f))$ and $R_{RX}/(R_{RX} + Z_{C,RC}(f))$ of the TX and the RX are no longer constant (Figs. 20 and 21) unlike in LC-dominant channels [26]. Therefore, the design tradeoffs caused by resistive terminations in RC-dominant channels and LC-dominant channels are different.

It is noticeable that the RC-dominance condition ($R \gg 2\pi f L$ and $2\pi f C \gg G$) depends on various factors: dimensions and materials of interconnects as well as operation frequencies. Regardless of its cross-sectional shape, whether a micro-strip line or a strip line, a typical RC-dominant channel is a scaled interconnect. For example, an interposer
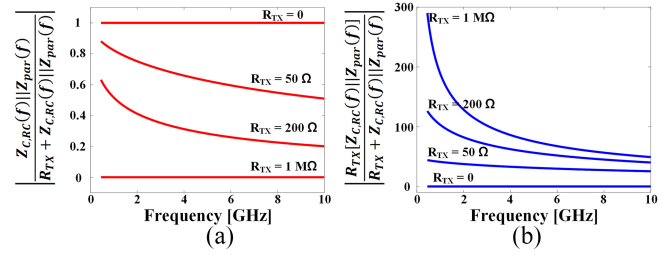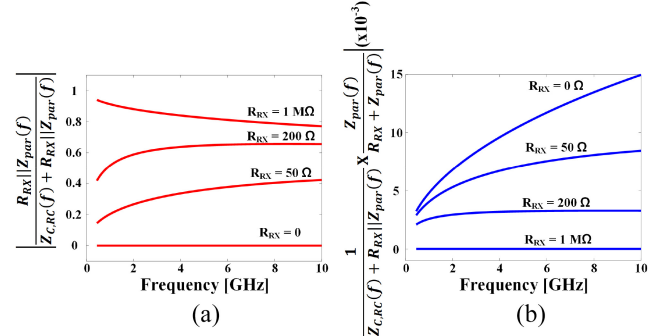

FIGURE 22. (a) TRX architecture for differential signaling. Simulated eye diagrams for two TX setups on RC-dominant channels: (b) TX with a 50-Ω termination driving a 10-mm channel at 5 Gb/s and (c) TX with a 10-Ω termination driving a 40-mm channel at 10 Gb/s [23].

wire or an on-chip wire that satisfies the RC-dominance condition is an RC-dominant channel. However, depending on the widths and spaces of lines as well as operating frequency, the scaled interconnects can be LC-dominant channels, too.

B. LOW-IMPEDANCE VOLTAGE-MODE TX

In RC-dominant applications, a low-impedance voltage-mode TX is preferred to the high-impedance current-mode TX [26] for larger amplitude and wider bandwidth. This can be understood by comparing the interconnect-TX interaction terms of voltage-mode and current-mode TXs. These

FIGURE 23. TRX architecture with charge-injection TX and a TIA termination at RX [25].

TABLE 3. Static dc currents consumed by a resistor termination and a TIA termination [25].

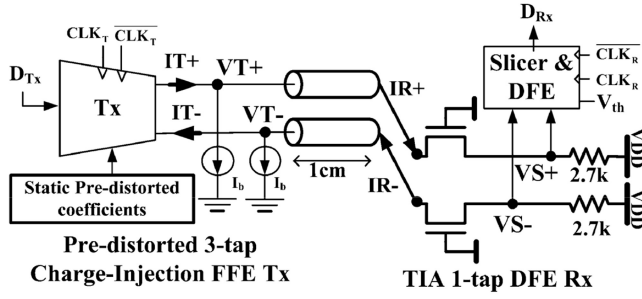|	**Resistor Termination**	**TIA Termination**
Input Impedance	860 Ω	860 Ω (small signal input impedance)
Bandwidth	53 MHz	53 MHz
Transimpedance (Gain)	860 Ω	2.7 kΩ
Static DC current	320 μA	160 μA

FIGURE 24. Various performance metrics versus RX termination impedance: circle markers for TIA termination and square markers for resistive termination with matching bandwidth [25].

FIGURE 25. TRX architecture with the FFE-combined crosstalk cancellation (XTC) and a TIA termination at RX [27].

terms are $(Z_{C,\mathrm{RC}}(f)||Z_{\mathrm{par}}(f))/(R_{\mathrm{TX}} + Z_{C,\mathrm{RC}}(f)||Z_{\mathrm{par}}(f))$ for a voltage-mode TX, and $R_{\mathrm{TX}}[Z_{C,\mathrm{RC}}(f)||Z_{\mathrm{par}}(f)]/(R_{\mathrm{TX}} + Z_{C,\mathrm{RC}}(f)||Z_{\mathrm{par}}(f))$ for a current-mode TX. These terms are modified from the interconnect-TX interaction terms in (9) and (10), assuming that the additional parasitic capacitor with an impedance of $Z_{\mathrm{par}}(f)$ is attached at the TX's output node. We do not need to consider the other terms of the transfer function for this comparison because they are independent of R_{TX}. With smaller R_{TX}, both the magnitude and the bandwidth are improved in a voltage-mode TX [Fig. 20(a)]. However, the bandwidth becomes very poor as R_{TX} increases for larger amplitude in a current-mode TX [Fig. 20(b)] because of the low-pass nature of $Z_{C,\mathrm{RC}}(f)$. As a result, a current-mode TX must sacrifice the bandwidth a lot for the signal amplitude, whereas the voltage-mode TX does not.

Kim et al. proposed a 10-Gb/s/ch low-impedance TX for a silicon carrier channel in [22] and [23]. The study showed that a 10-Ω TX with a 40-mm channel at 10 Gb/s achieved much larger eye opening at the TX output node than a 50-Ω TX with a 10-mm channel at 5 Gb/s (Fig. 22). However, a low-impedance TX requires larger transistors and more switching power consumption due to larger parasitic capacitances. For lower power consumption, a designer may use a small driver to implement a high-impedance TX while overcoming the poor bandwidth with FFE [22], [23].

C. DESIGN TRADEOFF IN VOLTAGE-MODE RX DESIGN

In a voltage-mode RX design for an RC-dominant application, high-impedance termination is preferred. To explain the
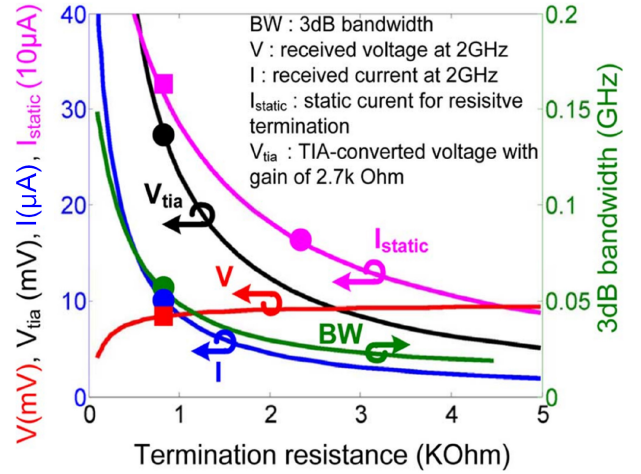
behavior with the impedance $Z_{\mathrm{par}}(f)$ of the parasitic capacitance at the RX's input node, the interconnect-RX interaction term is modified as $(R_{\mathrm{RX}}||Z_{\mathrm{par}}(f))/(Z_{C,\mathrm{RC}}(f) + R_{\mathrm{RX}}||Z_{\mathrm{par}}(f))$. The magnitude of the interaction term increases with a large R_{RX} [Fig. 21(a)].

A large R_{RX} also reduces the dc current from the RX termination to the TX through the interconnect [Fig. 22(a)] [23]. Because the power budget in RC-dominant applications is usually very tight, reducing the static dc current is very important. In [23], the static dc current is reduced from 4 to 0.2 mA by changing R_{RX} from 50 Ω to 1 kΩ for the same 0.8-V differential peak-to-peak swing (Table 4). However, the large R_{RX} also reduces the bandwidth [Fig. 21(a)], especially because the RX's input parasitic capacitance dominates R_{RX} at high frequency [Fig. 21(a)]. Kim et al. [23] compensated for the bandwidth

FIGURE 26. (a) TRX architecture with di-code interfaces. (b) Inverter-based TIA termination at RX [28].
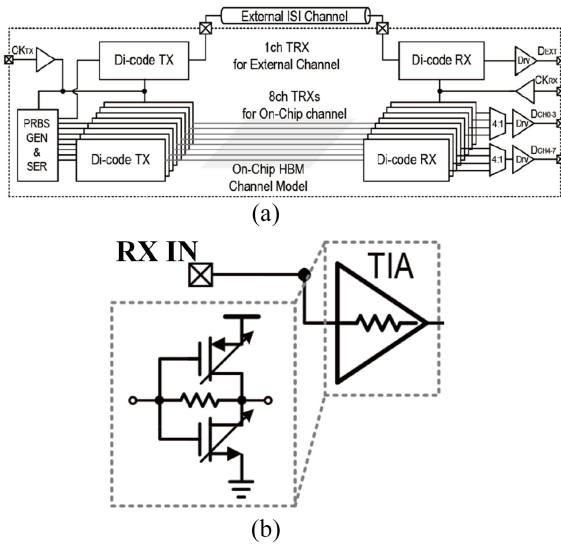
TABLE 4. Simple channel model.

Simplified Channel Model	$\dfrac{V_{RX}(l,f)}{V_{TX}(f)} \approx$ $\dfrac{Z_C(f)}{Z_{TX}(f)+Z_C(f)} 2e^{-l\gamma(f)} \dfrac{Z_{RX}(f)}{Z_C(f)+Z_{RX}(f)}$
Validity Condition	$\lvert \eta(f) \rvert = \lvert \Gamma_{TX}(f)\Gamma_{RX}(f)e^{-2l\gamma(f)} \rvert \ll 1$
Interconnect-TX Interaction	$\dfrac{Z_C(f)}{Z_{TX}(f)+Z_C(f)}$
Attenuation	$2e^{-l\gamma(f)}$
Interconnect-RX Interaction	$\dfrac{Z_{RX}(f)}{Z_C(f)+Z_{RX}(f)}$

TABLE 5. Comparison between *LC*-dominant and *RC*-dominant channels.

	LC-dominant	*RC*-dominant
Condition	$2\pi fL \gg R_s\sqrt{f}$, $2\pi fC \gg G_d f$	$R \gg 2\pi fL$, $2\pi fC \gg G$
Chacteristics	$Z_{C,LC}(f) \approx \sqrt{\dfrac{L}{C}}$, $\gamma_{LC}(f) \approx j2\pi\sqrt{LC}f + \dfrac{R_s}{2Z_{C,LC}}\sqrt{f} + \dfrac{G_d Z_{C,LC}}{2}f$	$Z_{C,RC}(f) \approx \sqrt{R/j2\pi fC}$, $\gamma_{RC}(f) \approx \sqrt{j2\pi fRC}$
Interconnect Types	Cables, backplane traces, PCB traces, organic packages, interposers, on-chip wires	interposers, on-chip wires

reduction by introducing a 10-Gb/s compact and energy-efficient DFE utilizing an infinite impulse response (IIR) filter.

D. DESIGN TRADEOFF IN CURRENT-MODE RX DESIGN

In current-mode RX design, low-impedance termination is preferred because both the magnitude and the bandwidth of the interconnect-RX interaction term $Z_{par}(f)/\{(Z_{C,RC}(f) + R_{RX}\lvert\lvert Z_{par}(f)) \cdot (R_{RX} + Z_{par}(f))\}$ increase with smaller R_{RX} [Fig. 21(b)]: the interconnect-RX interaction term is modified with a parasitic capacitance $Z_{par}(f)$ at the RX output node. However, the static dc current increases with smaller R_{RX}. Therefore, more static power must be consumed for a wider bandwidth and a larger amplitude [26].

E. TIA-TERMINATION TECHNIQUES FOR THE RX

In RC-dominant applications, a TIA termination provides both advantages of the voltage-mode and the current-mode RXs [24], [25] (Fig. 2). This approach breaks the direct dependency of the current gain on the RX's input impedance

and the static current. In Fig. 23, the RX termination impedance R_{RX} ($\approx 860~\Omega$) is set small by the small signal input impedance of the TIA for good bandwidth (54 MHz) while the static current is limited small (160 μA) by the bias current sources (I_b) at the TX to reduce static dc power consumption. The small R_{RX} enhances the amplitude of the input current and the bandwidth while reducing the amplitude of the input voltage and increasing the static power consumption. The large input current is converted to voltage for sensing by the TIA gain of 2.7 kΩ. The converted voltage amplitude (V_{RX}) is three times higher than the one with the pure resistive $R_{RX} = 860~\Omega$ for the same bandwidth (Fig. 24). Using the pure resistive R_{RX}, the same current–voltage conversion gain of 2.7 kΩ can be achieved at $2\times$ static power and half bandwidth. As a result, energy-efficient wireline communication of 4–6-Gb/s data rates can be achieved via an RC-dominant channel while consuming 0.356–0.635 pJ/b, respectively. Table 3 compares the static dc current consumptions when the RX is terminated by a resistor and a TIA for the same channel bandwidth [24], [25]. Therefore, in the current-mode RX, a TIA termination achieves three key benefits simultaneously: 1) wide bandwidth; 2) large signal amplitude; and 3) low static power consumption. The TIA termination accomplishes these benefits by separating the small signal input impedance from the output trans-impedance gain.

The principle of the TIA termination technique can be implemented with various modifications. Ko et al. [27] proposed an RX termination technique with a regulated-cascode TIA for high-loss HBM on silicon interposer applications. This article shows 4-Gb/s/ch TRXs for HBM on a silicon interposer (Fig. 25) and a TIA circuit that reduces the input impedance of the RX by feedback in order to increase the bandwidth of the channel. Park et al. proposed to use a simple inverter-based TIA termination for HBM interfaces based on di-code signaling (Fig. 26). The inverter-based TIA was used for dc balancing of di-code signaling while a 10-Gb/s/ch di-code output driver is used at the TX [28].

TABLE 6. Resistive termination techniques for LC-dominant channels.

	Imepedance Matching	Single-Sided Termination	Adaptive Relaxed Impedance Matching	Impedance Mismatch with Reflection Cancellation
Termination Condition	$R_{TX} = R_{RX} = Z_0$	$R_{TX} = Z_0$ or $R_{RX} = Z_0$	$\|\eta(f)\| = \|\Gamma_{TX}(f)\Gamma_{RX}(f)e^{-2t\gamma(f)}\| \ll 1$	$R_{TX} \neq Z_0$ and $R_{RX} \neq Z_0$
Reflection	Absorption at TX and RX	Absorption at Only TX or Only RX	Controlled below a designed level	Canceling by Equalization
Advantage	Best Signal Integrity, Simple Design	Improved Signal Swing or Power Efficiency, Simple Design	Improved Signal Swing or Power Efficiency, Seamless Compatibility with Various Impedances	Improved Signal Swing or Power Efficiency
Limitation	Best Signal Integrity	Reduced Signal Integrity	Reduced Signal Integrity, Adapation Complexity	Equalization Complexity

TABLE 7. Resistive termination techniques for RC-dominant channels.

Termination Circuit Types	Preferred Impedance	Advantage	Disadvantage
Voltage-Mode TX	Low Impedance	Large Amplitude Wide Bandwidth	Increased Static Current
Current-Mode TX	High Impedance	Large Amplitude	Narrow Bandwidth
Voltage-Mode RX	High Impedance	Large Amplitude Reduce Static Current	Narrow Bandwidth
Current-Mode RX	Low Impedance	Lage Amplitude Large Static Current	Wide Bandwdith
TIA-RX	Low Input Impedance	Wide Bandwidth Large Amplitude Small Static Current	Increased Design Complexity
	High Transimpedance Gain		

V. CONCLUSION

This article has reviewed resistive termination techniques for wireline applications, focusing on their impact on channel behaviors. We presented an intuitive analytical model to understand how termination resistances affect channel characteristics (Table 4), and explained the different characteristics of LC-dominant and RC-dominant channels (Table 5). For LC-dominant channels, we reviewed techniques like relaxed impedance matching, which enables design improvements beyond traditional 50-Ω constraints (Table 6). In RC-dominant applications, we highlighted how termination strategies can differ from the ones in LC-dominant applications (Table 7). Our analysis emphasizes the importance of carefully designing termination impedances for specific applications, considering both channel behaviors and overall link performance. As wireline technology advances, these termination techniques offer significant potential for improving link performance and power efficiency.

ACKNOWLEDGMENT

REFERENCES

[1] H. Johnson and M. Graham, *High-Speed Signal Propagation: Advanced Black Magic*. Upper Saddle River, NJ, USA: Prentice Hall, 2003.

[2] M. Choi, J.-Y. Sim, H.-J. Park, and B. Kim, "An approximate closed-form channel model for diverse interconnect applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 10, pp. 3034–3043, Oct. 2014.

[3] E. Sayre, "Understanding skin effect and dielectric loss material effects on digital interconnects," in *Proc. DesignCon*, Santa Clara, CA, USA, 2018, pp. 1–14.

[4] A. Deutsch, "Electrical characteristics of interconnections for high-performance systems," *Proc. IEEE*, vol. 86, no. 2, pp. 315–355, Feb. 1998.

[5] S. Ramo and J. R. Whinnery, *Fields and Waves in Modern Radio*. New York, NY, USA: Wiley, 1944.

[6] M. Choi, K. Kim, J.-Y. Sim, H.-J. Park, and B. Kim, "Analytical formulas for tradeoff among channel loss, length, and frequency of *RC*-and *LC*-dominant single-ended interconnects for fast equalized link tradeoff estimation," *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 5, no. 10, pp. 1497–1506, Oct. 2015.

[7] J. Kim et al., "8.1 a 224Gb/s DAC-based PAM-4 transmitter with 8-Tap FFE in 10nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2021, pp. 126–128.

[8] Y. Segal et al., "A 1.41pJ/b 224Gb/s PAM-4 SerDes receiver with 31dB loss compensation," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2022, pp. 114–116.

[9] Y. Wei et al., "9.3 NVLink-C2C: A coherent off package chip-to-chip interconnect with 40 Gbps/pin single-ended signaling," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2023, pp. 160–161.

[10] J. Wilson et al., "A 1.17pJ/b 25Gb/s/pin ground-referenced single-ended serial link for off-and on-package communication in 16nm CMOS using a process-and temperature-adaptive voltage regulator," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2018, pp. 276–277.

[11] J. W. Poulton et al., "A 0.54pJ/b 20Gb/s ground-referenced single-ended short-haul serial link in 28nm CMOS for advanced packaging applications," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2013, pp. 404–405.

[12] M. Choi et al., "An FFE TX with 3.8x eye improvement by automatic impedance adaptation for universal compatibility with arbitrary channel and RX impedances," in *Proc. IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2017, pp. 58–59.

[13] M. Choi et al., "An FFE transmitter which automatically and adaptively relaxes impedance matching," *IEEE J. Solid-State Circuits*, vol. 53, no. 6, pp. 1780–1792, Jun. 2018.

[14] M. Lee, P. K. Kaur, J. Seo, S. Han, and B. Kim, "A compact single-ended inverter-based transceiver with swing improvement for short-reach links," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 69, no. 9, pp. 3679–3688, Sep. 2022.

[15] C. Moon, J. Seo, M. Lee, I. Jang, and B. Kim, "A 20 Gb/s/pin 1.18pJ/b 1149μm^2 single-ended inverter-based 4-tap addition-only feed-forward equalization transmitter with improved robustness to coefficient errors in 28nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2022, pp. 450–451.

[16] C. Moon, J. Seo, M. Lee, I. Jang, and B. Kim, "A single-ended inverter-based addition-only feed-forward equalization transmitter," *IEEE J. Solid-State Circuits*, vol. 59, no. 11, pp. 3741–3751, Nov. 2024, doi: 10.1109/JSSC.2024.3397046.

[17] B. Dehlaghi and A. C. Carusone, "A 0.3 pJ/bit 20 Gb/s/Wire parallel interface for die-to-die communication," *IEEE J. Solid-State Circuits*, vol. 51, no. 11, pp. 2690–2701, Nov. 2016.

[18] J. Jin et al., "A 4nm 16Gb/s/pin single-ended pam4 parallel transceiver with switching-jitter compensation and transmitter optimization," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2023, pp. 404–405.

[19] J. Jin et al., "A 4-nm 16-Gb/s/pin single-ended PAM-4 parallel transceiver with switching-jitter compensation and transmitter optimization," *IEEE J. Solid-State Circuits*, vol. 59, no. 1, pp. 184–195, Jan. 2024.

[20] S.-M. Lee et al., "A % reduction in transceiver power for single-ended point-to-point DRAM interface with the termination resistance of $4 \times Z_0$ at both TX and RX," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2013, pp. 308–309.

[21] K. Seong et al., "A 4nm 32Gb/s 8Tb/s/mm die-to-die chiplet using NRZ single-ended transceiver with equalization schemes and training techniques," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2023, pp. 114–115.

[22] Y. Liu, B. Kim, T. O. Dickson, J. F. Bulzacchelli, and. D. Friedman, "A 10-Gb/s compact low-power serial I/O with DFE-IIR equalization in 65-nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2009, pp. 182–183.

[23] B. Kim, Y. Liu, T. O. Dickson, J. F. Bulzacchelli, and. D. Friedman, "A 10-Gb/s compact low-power serial I/O with DFE-IIR equalization in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3526–3538, Dec. 2009.

[24] B. Kim and V. Stojanović, "A 4Gb/s/ch 356fJ/b 10mm equalized on-chip interconnect with nonlinear charge-injecting transmit filter and transimpedance receiver in 90nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2009, pp. 66–67.

[25] B. Kim and V. Stojanović, "An energy-efficient equalized transceiver for RC-dominant channels," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1186–1197, Jun. 2010.

[26] M. Choi, J.-Y. Sim, H.-J. Park, and B. Kim, "A channel model of scaled RC-dominant wires for high-speed wireline transceiver design," *J. Semicond. Technol. Sci.*, vol. 13, no. 5, pp. 482–491, Oct. 2013.

[27] H.-G. Ko, S. Shin, J. Oh, K. Park, and D.-K. Jeong, "An 8Gb/s/um FFE-combined crosstalk-cancellation scheme for HBM on silicon interposer with 3D-staggered channels," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2020, pp. 128–129.

[28] H. Park et al., "A 0.385-pJ/bit 10-Gb/s TIA-terminated di-code transceiver with edge-delayed equalization, ECC, and mismatch calibration for HBM interfaces," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2022, pp. 452–453.

MINSOO CHOI (Member, IEEE) received the B.S. degree in electronic engineering from Soongsil University, Seoul, South Korea, in 2012, and the M.S. and Ph.D. degrees in electrical engineering from the Pohang University of Science and Technology, Pohang, South Korea, in 2014 and 2018, respectively.

From 2018 to 2020, he was with the University of California at Berkeley, CA, USA, as a Postdoctoral Researcher. From 2021 to 2024, He worked with Samsung Semiconductor, Inc., San Jose, CA, USA. He is currently a Senior Staff Engineer with the Optical PHY team, Marvell Technology, Santa Clara, CA, USA.

MYUNGGUK LEE received the B.S. degree in electronic engineering from the Kumoh National Institute of Technology, Gumi, South Korea, in 2015, and the M.S. and Ph.D. degrees in electrical engineering from the Pohang University of Science and Technology, Pohang, South Korea, in 2017 and 2024, respectively.

In 2024, he become a Staff Engineer with the Standard HBM Group, Samsung Electronics, Hwaseong, South Korea.

BYUNGSUB KIM (Senior Member, IEEE) received the B.S. degree in electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, South Korea, in 2000, and the M.S. and Ph.D. degrees in electrical engineering and computer science from Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, in 2004 and 2010, respectively.

He was an Analog Design Engineer with Intel Corporation, Hillsboro, OR, USA, from 2010 to 2011. In 2012, he joined the faculty of Department of Electrical Engineering, POSTECH, where he is currently a Professor with the Department of Convergence IT Engineering and the Department of Semiconductor Engineering. He is currently a Professor with the Institute for Convergence Research and Education in Advanced Technology, Yonsei University, Seoul, South Korea.

Dr. Kim received several honorable awards. He was a recipient of the IEEE Journal of Solid-State Circuits Best Paper Award, in 2009, the Analog Device Inc., and the Outstanding Student Designer Award from MIT, in 2009. He was a co-recipient of the Beatrice Winner Award for Editorial Excellence at the 2009 IEEE International Solid-State Circuits Conference. For several years, he served or has been serving as the Technical Program Committee Member of the IEEE International Solid-State Circuits Conference and the IEEE Asian Solid-State Circuit Conference.

CHANGJAE MOON (Graduate Student Member, IEEE) received the B.S. degree in electronic and electrical engineering from the Pohang University of Science and Technology, Pohang, South Korea, in 2018, where he is currently pursuing the combined M.S.–Ph.D. degree.

His research interests include high-speed links and signal integrity.